FormFactor™

Advancing Probe Card Parallelism for SOC Devices

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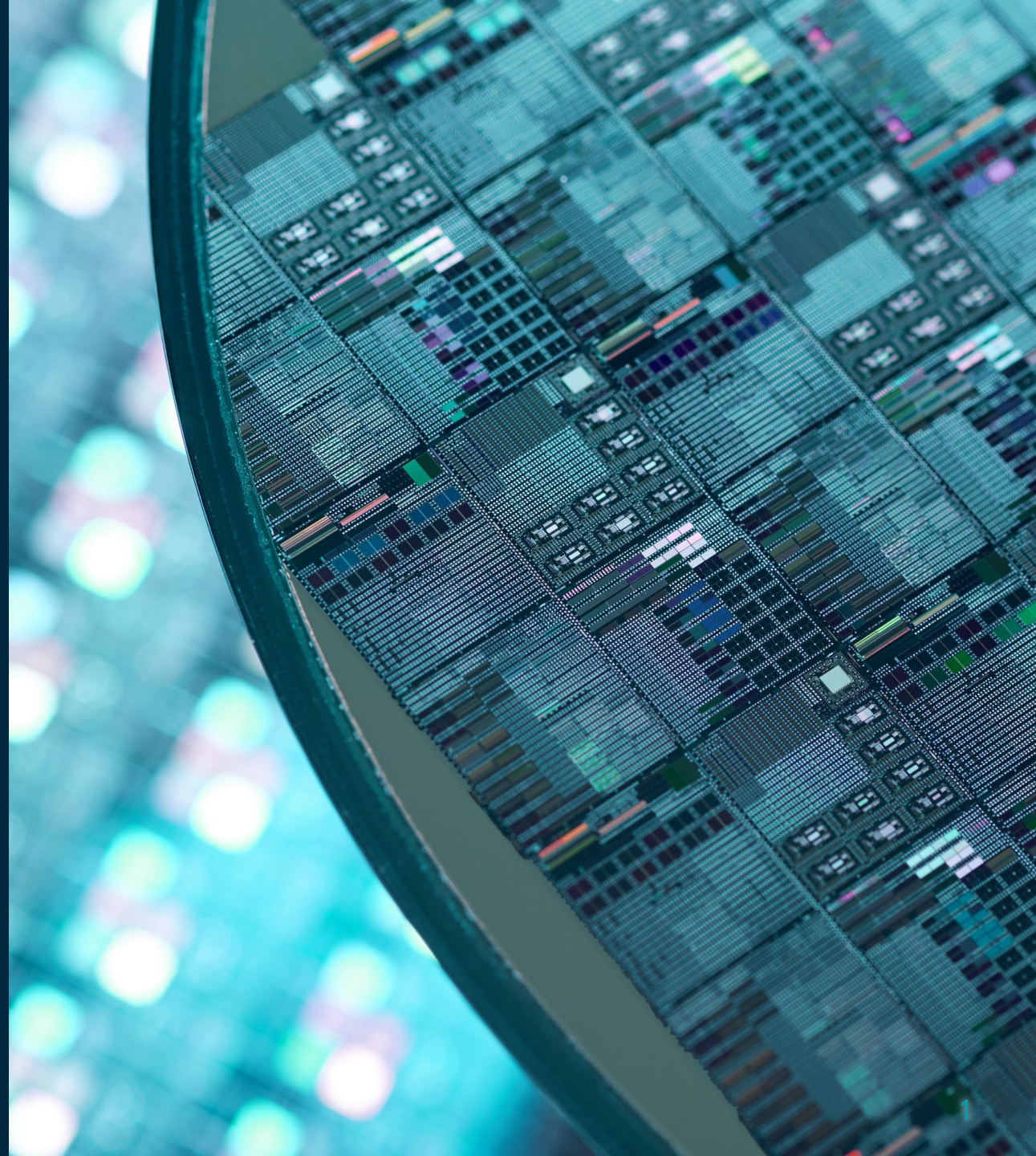
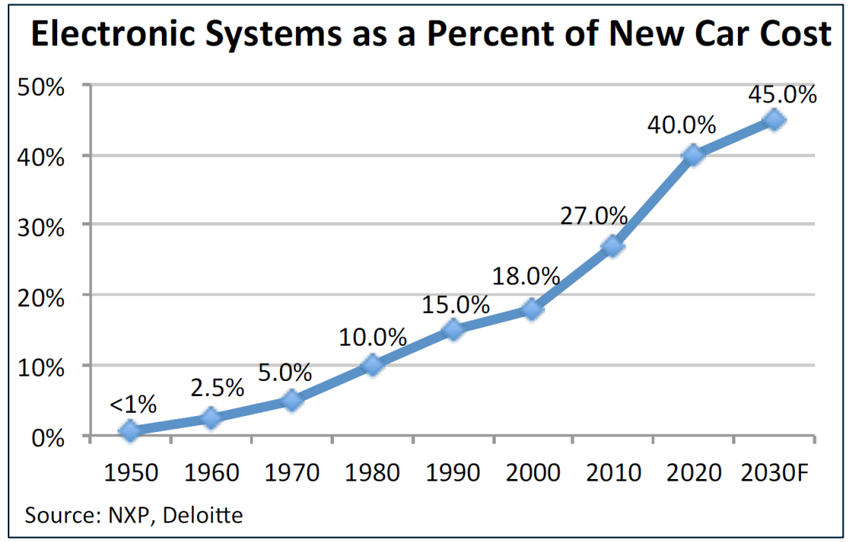


Overview

- Automotive Semiconductor Market Overview
- Project Motivation and Incentives
- Touchdown Analysis and Comparison
- True Scale Matrix Overview
- True Scale Matrix Test and Qualification Results
- Summary

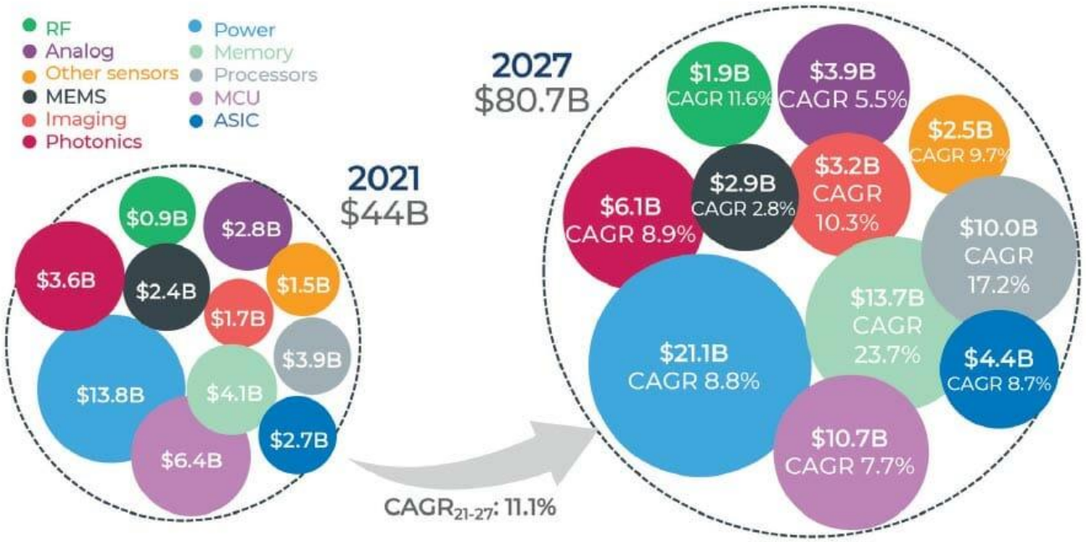
Automotive Semiconductor Market Overview

- Automotive electronics is one of the highest growth segments in the market
  - Semiconductor-built electronics is expected to approach nearly **half the cost of a new car** early next decade.
  - In 2021 Automotive IC Market size increased to **~$44B**
  - Expanding at a CAGR of **11.1%** from 2021 to 2027



2021-2027 semiconductors for automotive market forecast

(Source: Semiconductor Trends in Automotive 2022, Yole Intelligence, 2022, October 2022)



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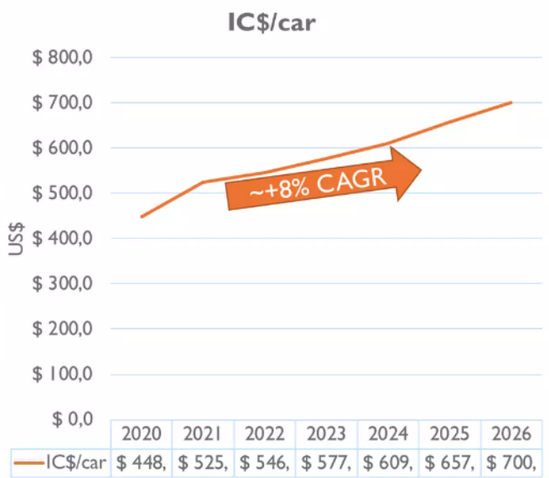
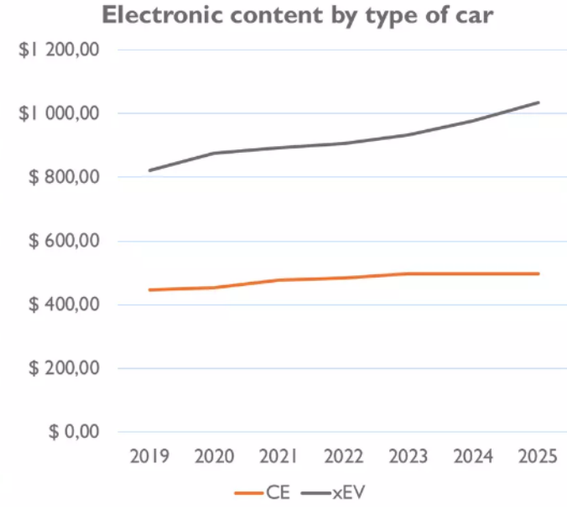
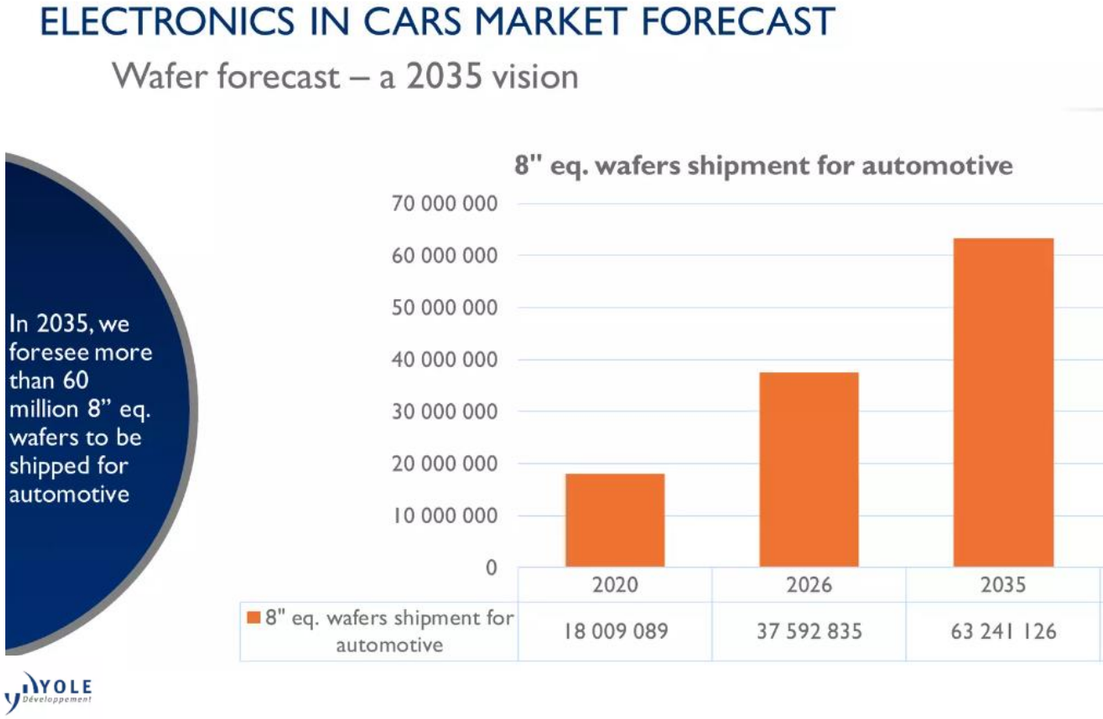




Automotive Semiconductor Trends 2021

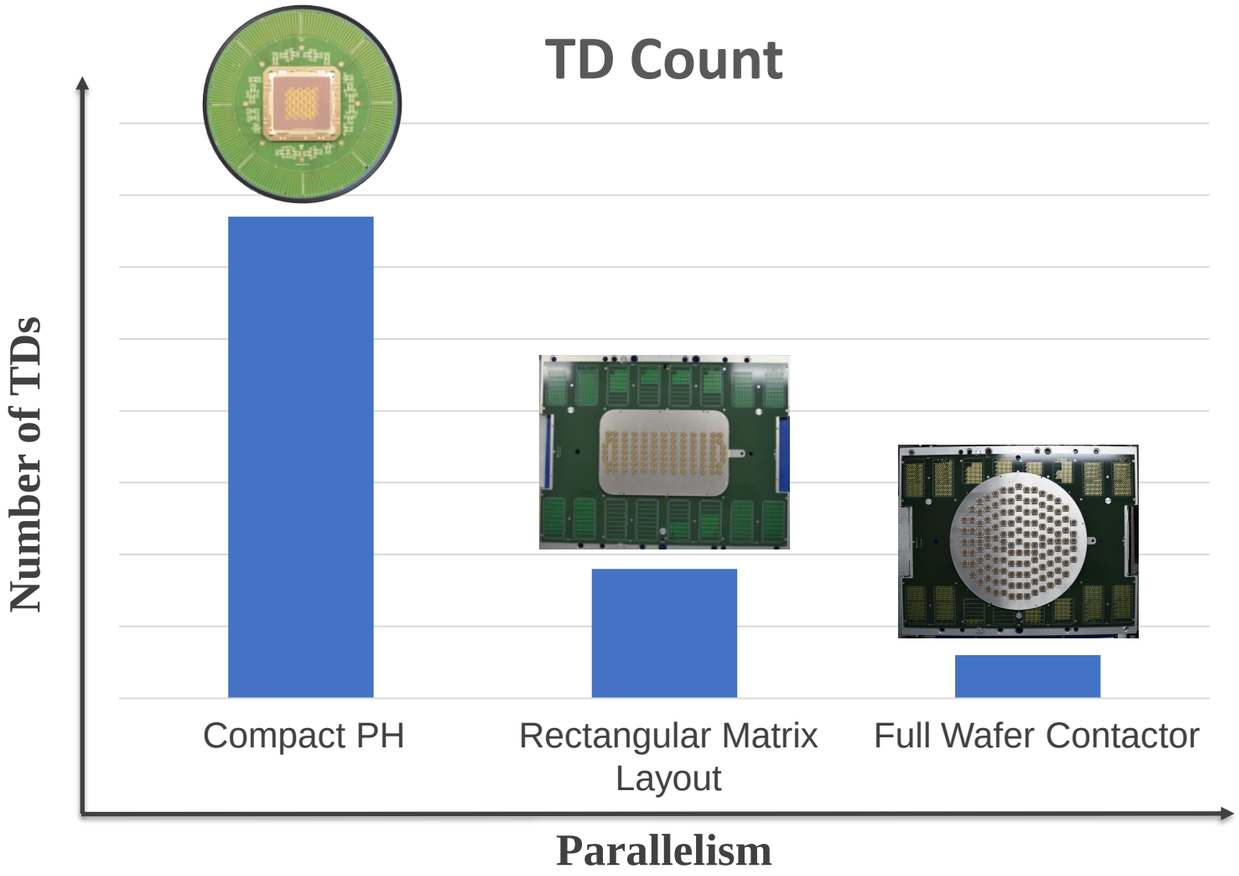
Project Motivation

- World-wide demand of semiconductor is driving significant growth, specifically due to decarbonization and digitalization
  - Semiconductor suppliers forecasted to increase wafer output for automotive ICs by 52% from 2020 to 2026 with a CAGR of 8.7% (’20-’35)
- **Key project goals:**
  - Increase throughput in wafer test with limited tester
  - Decrease test costs per die
- Challenges:
  - Hourly rate for test cost is increasing
  - Allocation of further test capacity blocked by global supply chain issues
- Consequence for wafer test:
  - Increase the parallelism at wafer test without increase of tester resources by……
    - Optimizing test strategy (modular test insertions)
    - Optimizing the usage of available tester resources (DPS, channels)



Parallelism vs Touchdown

- Increased tester resources introduces the opportunity to raise the parallelism.
- Raising the parallelism would help to reduce the number of required TDs in order to test an entire wafer.
- Number of required TDs for each wafer directly impacts the test time/cost.



As number of sites tested on each TD increases, the test time per wafer significantly decreases

Touchdown-Efficiency Analysis

- Increase of parallelism is the preferred method to reduce test costs and increase the throughput by decreased TD per wafer and saving time.

- Touchdown-Efficiency (TDE) is a value for the efficiency usage of the full tester resources, for which the probe card is responsible

TDE: Touchdown-efficiency

$N_{Sites\ Max}$: Number of maximum available sites, based on tester resources

N_{TD} : Number of Touchdowns per wafer

N_{Dies} : Number of Dies to test on the wafer

$$TDE = \frac{N_{Dies}}{N_{TD} * N_{Sites\ Max}} * 100\%$$

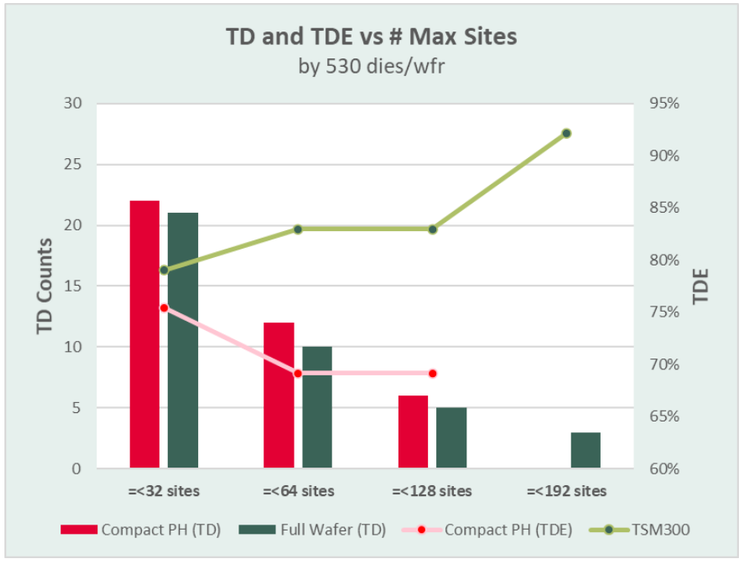
- For example, if there are 3000 Dies on a wafer and your tester can support resources for max 500 sites:

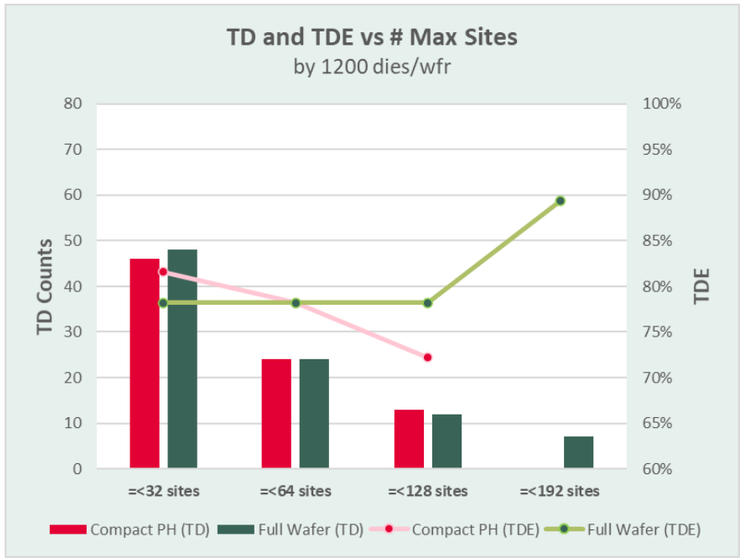
A PC with 8 TD → **TDE = 75%**

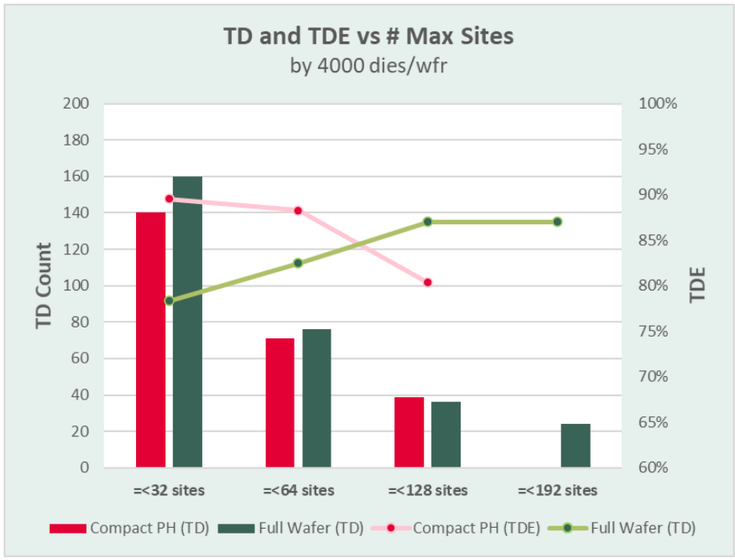
$$TDE = \frac{3000}{8 * 500} * 100\% = 75\%$$

TD Count and Efficiency Gains with Full Wafer Contactor (FWC)

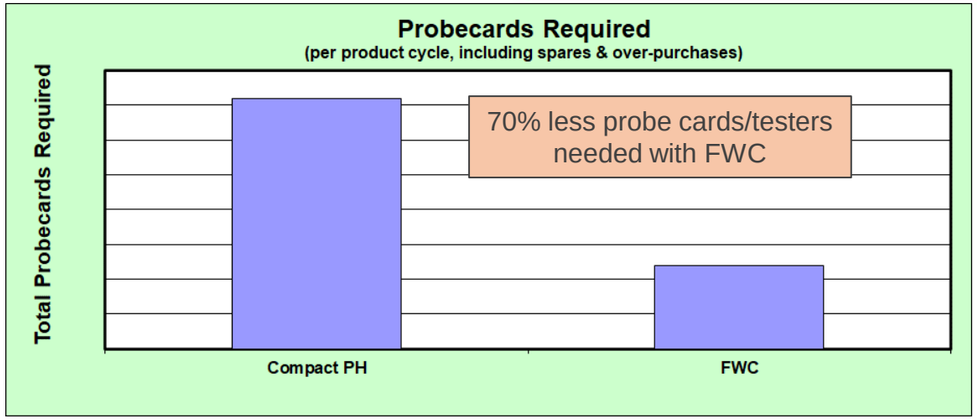
- TDE depends on different parameters:
  - Wafer → Number of Dies to be tested on wafer
  - Tester → Number of maximum available sites, based on tester resources
  - Probe card → Number of required TD to cover the wafer

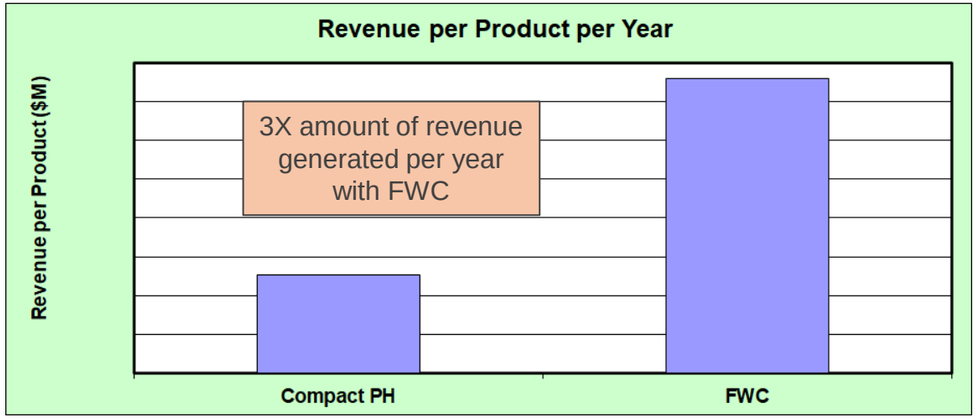


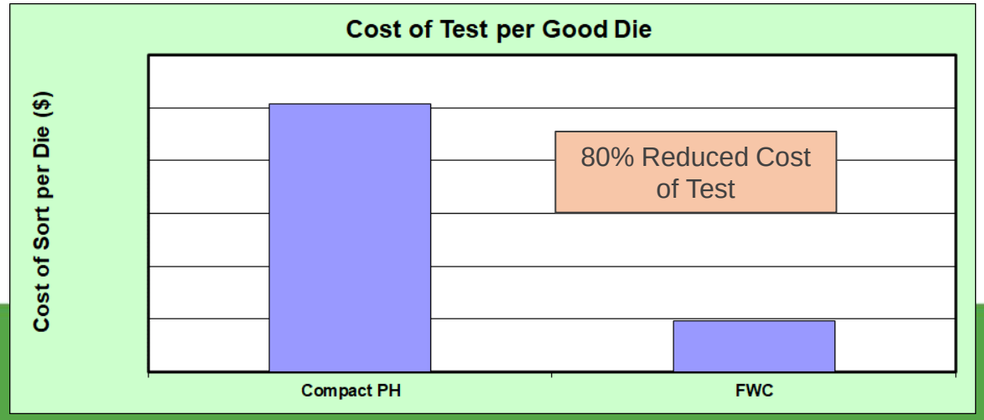




Full wafer contactors enables best TDE with highest parallelism





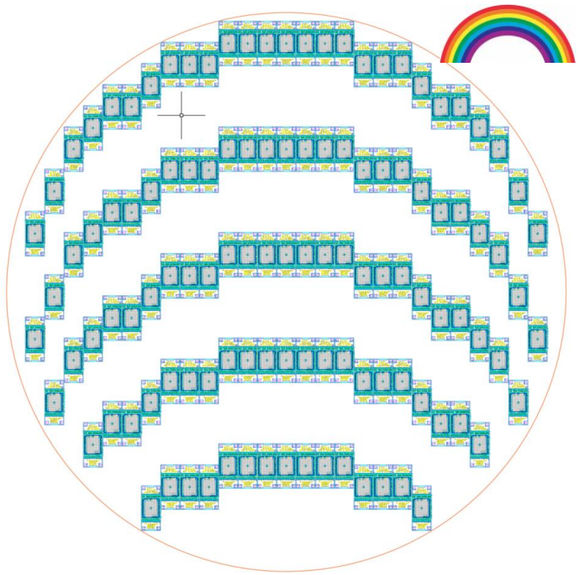


Cost of Test Model and Analysis

- Major motivation was to maximize throughput with limited tester availability
  - Evaluated throughput increase
    - x64 solid array → 24 TD
    - x192 FWC → 7 TD
- Model assumptions
  - 1184 die per wafer
  - 180 sec TD for each PH option
  - 2500 wafer starts per month
  - Only 2 test cells available – not able to increase
  - Wafer and Package yield, maintenance and other parameters are assumed similar on both scenarios for model simplicity
- Conclusion:
  - Model confirms the **full wafer contactor can support project goals** to **increase test cell throughput** without significant additional capital expenditures and **reduce overall cost of tested die**

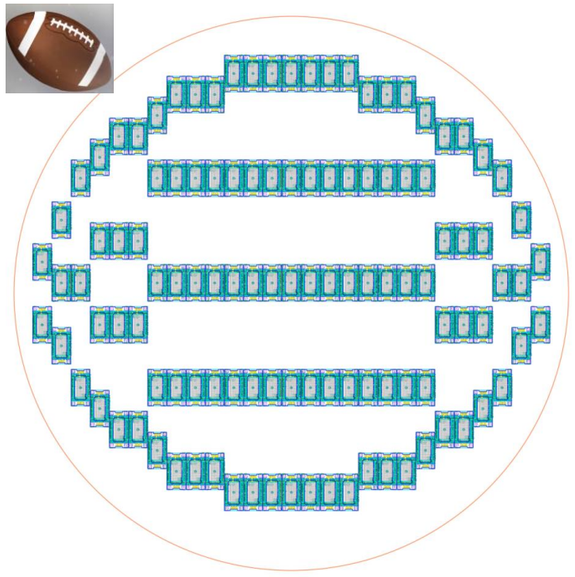
Full Wafer Contactor Array – Optimized Site Arrangement

- Allows the placement of a very high number of site
- The array can be optimized based on priorities
- Enables thermally stable conditions – low rate of stepping off the wafer
- No chuck deflection at high pin count probecards – well distributed contact force across wafer



Rainbow vs Football

(Both are experts in TDs)

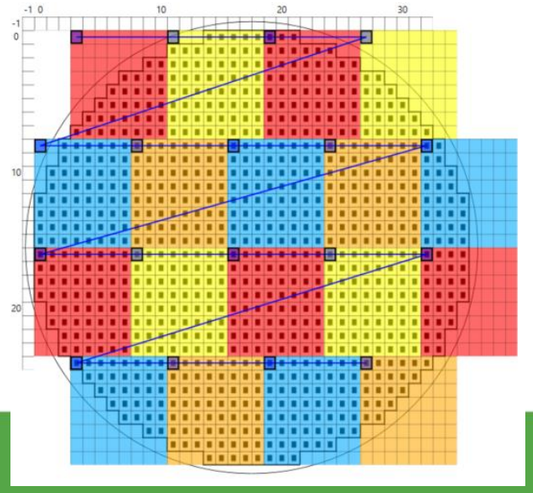


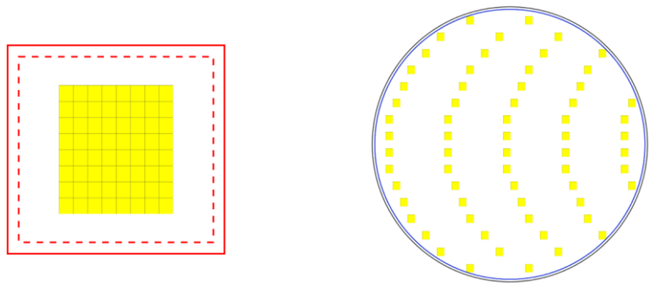
✓ No overlapping of TDs
? Larger tip boundary, less space for cleaning TDs

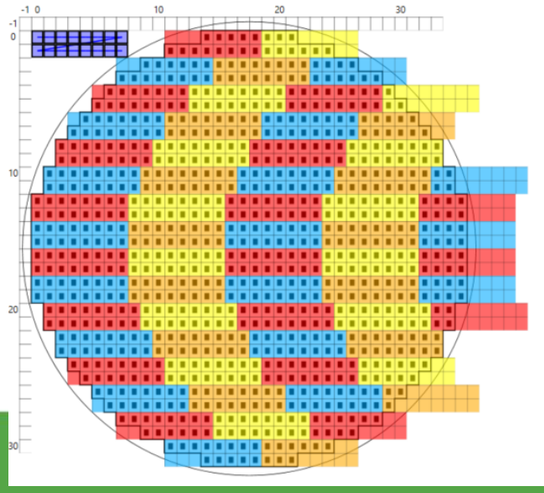
✓ Smaller tip boundary, more space for cleaning TDs
✓ Better contact force distribution
✓ Less stepping outside of the wafer
? Overlapping TDs is required in most cases

Thermal Condition Improvement During TDs

- The thermal behavior of a probe card with any array is very critical for TDs at the wafer edge
- The partial touchdowns on edge can impact the performance of the card depending on:
  - Temperature of the test
  - Test time for each TD
  - Number of consecutive partial TD
- Full wafer array has improved stable thermal condition due to lower rate of stepping out of wafer compared to a compact array
  - Rainbow: Up to 90% of the springs are touching the wafer
  - Football: Up to 98% of the springs are touching the wafer

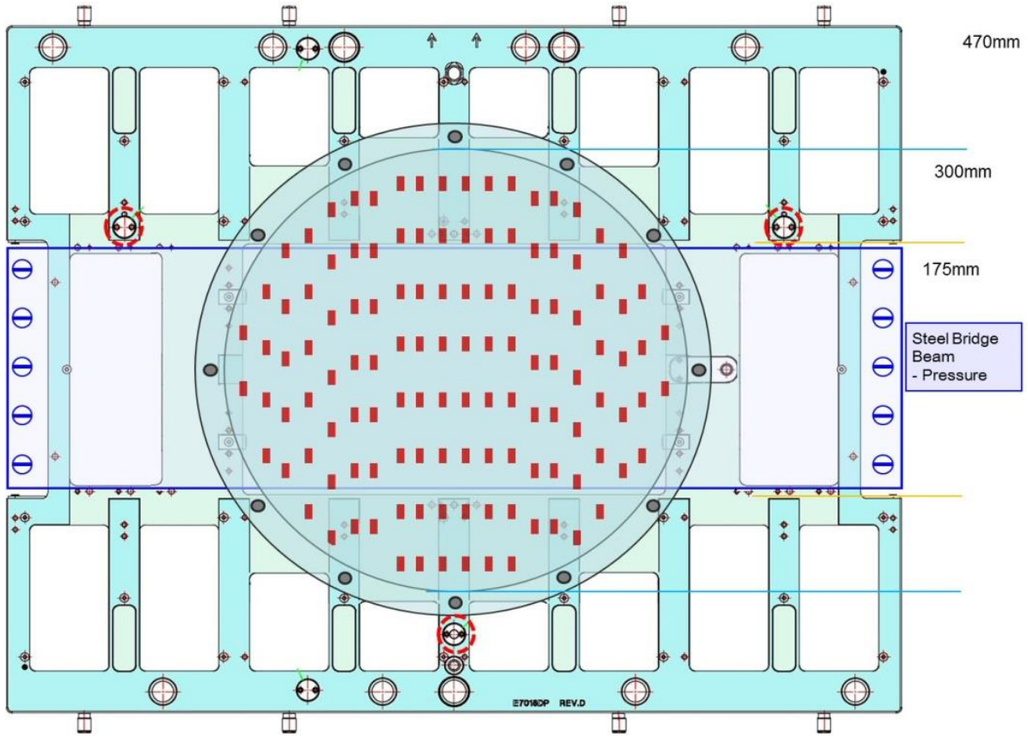


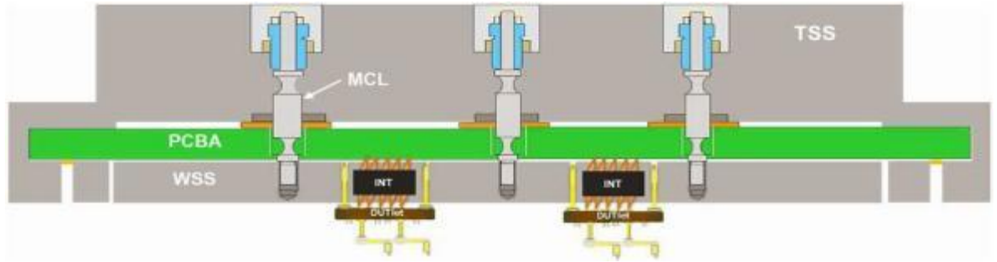


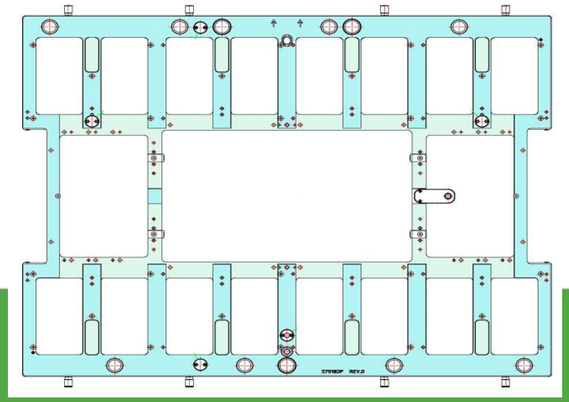


Probe Card Requirements and Challenges

- **High parallel probe card on V93K Direct-Dock**
  - Probe Card active area limit to V93K standard stiffener
    - Tester side stiffener re-design is needed
  - Largest probing area on V93K platform
    - Robust mechanical design is requested to prevent Z direction deflection force when probing.
  - Wide Range Temp Test (-40ºC to 150ºC)
    - Special WSS material can be chosen for desired thermal expansion properties
    - For dual temp applications, can be matched to that of silicon – probe tips more accurately track pads across temp. range

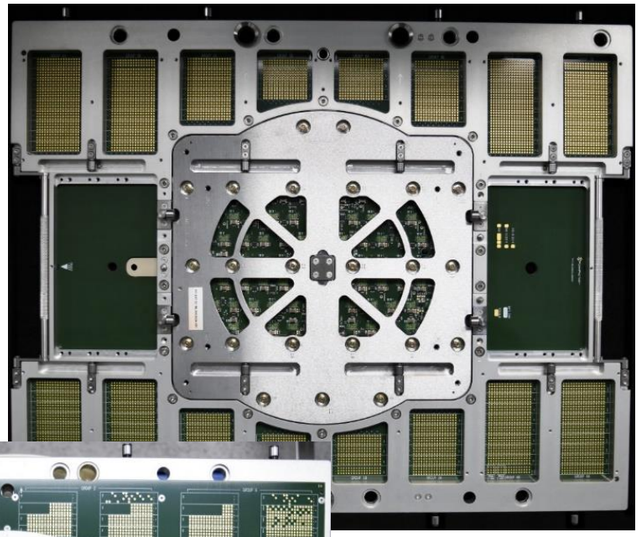


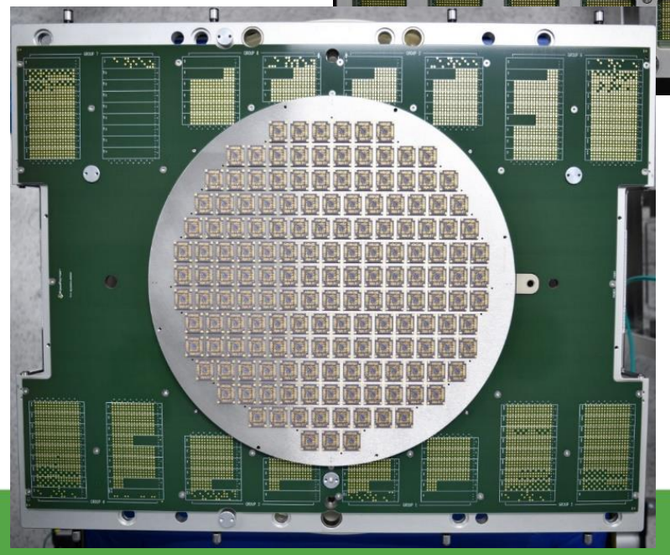




FFI TrueScale Matrix for Full Wafer Contactor Probing

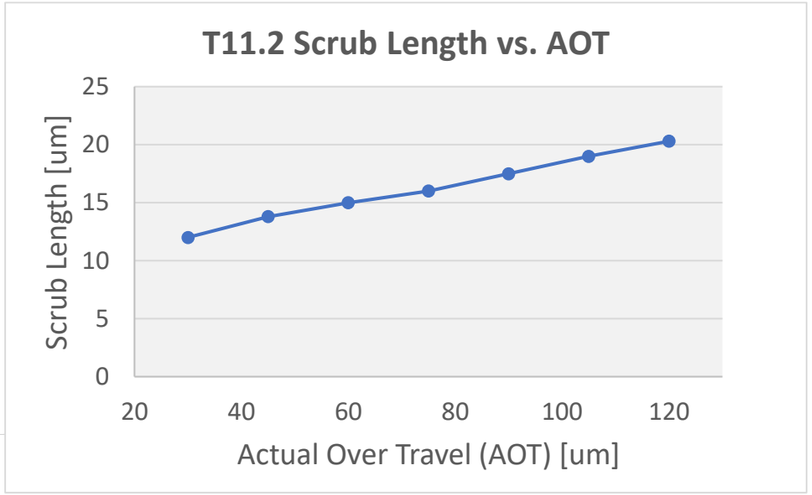
- FormFactor TrueScale Matrix FWC solution for DD tester configurations
  - Based on FFI production proven Matrix full wafer contactor platform
  - Design modifications to both inner TSS and outer TSS
  - Depopulated pogo bank configuration in the test head
- Target Devices/Application space
  - SOC device, peripheral pads down to 60um pad pitch, pad size down to 48um
  - Wide temp. range from -40ºC to 150ºC temperature range
- **High parallelism full wafer contactor**
  - Utilize low force T11 MEMS springs
  - 50K+ probe count capability
  - Increased parallelism – over 200 sites
  - Thermally stable architecture to support very wide temperature range capability
    - Meets -40ºC to 150ºC testing requirements

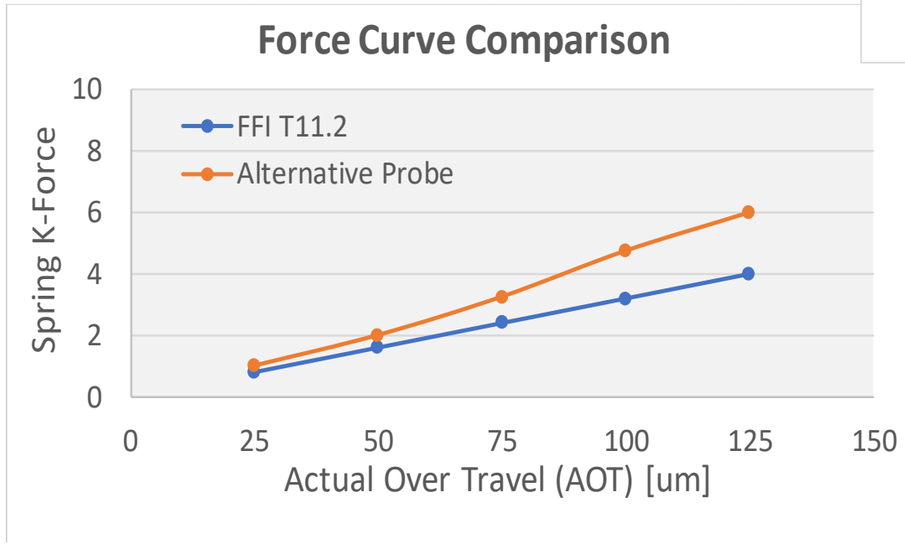


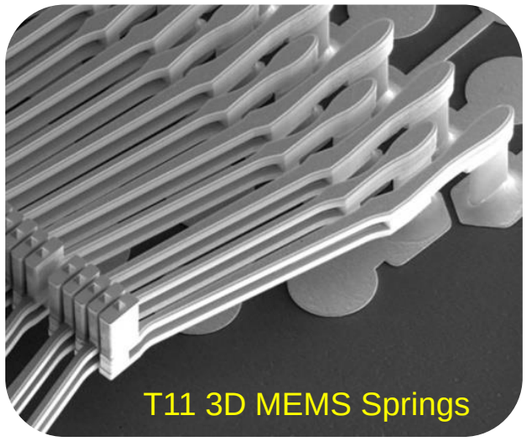


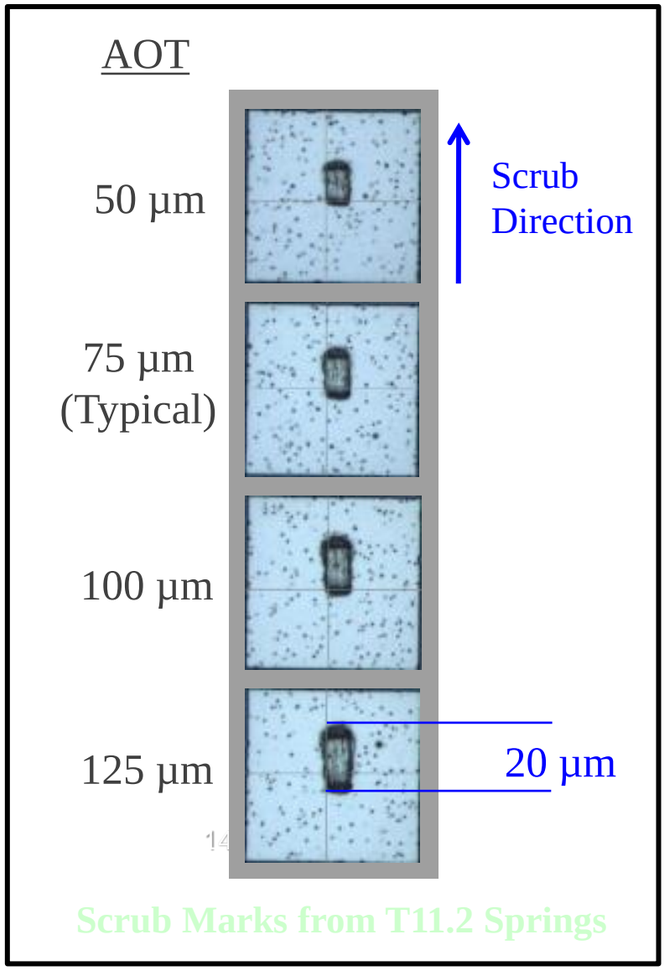
FFI T11.2 3D MEMS Springs

- Low force springs
- Small scrub marks
- Minimized pad impact



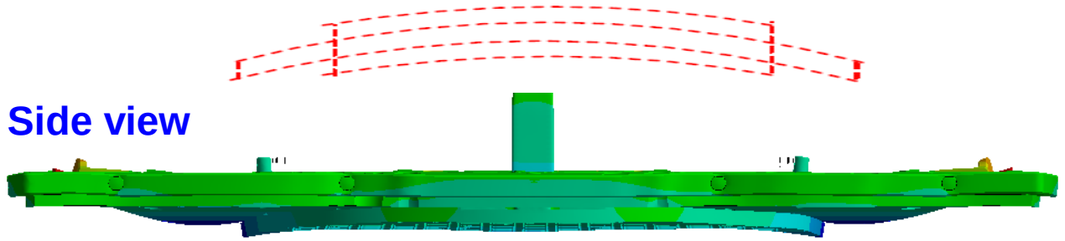




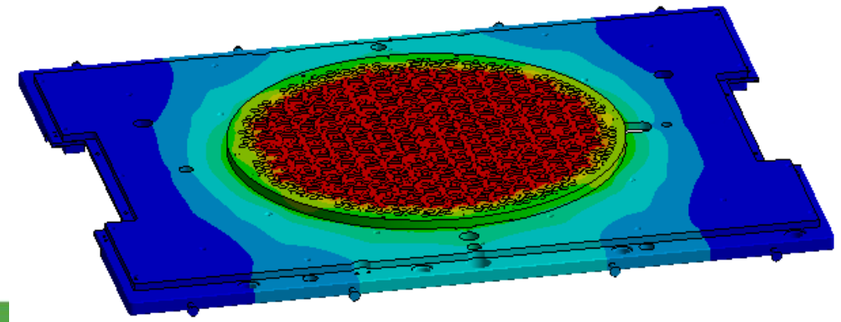


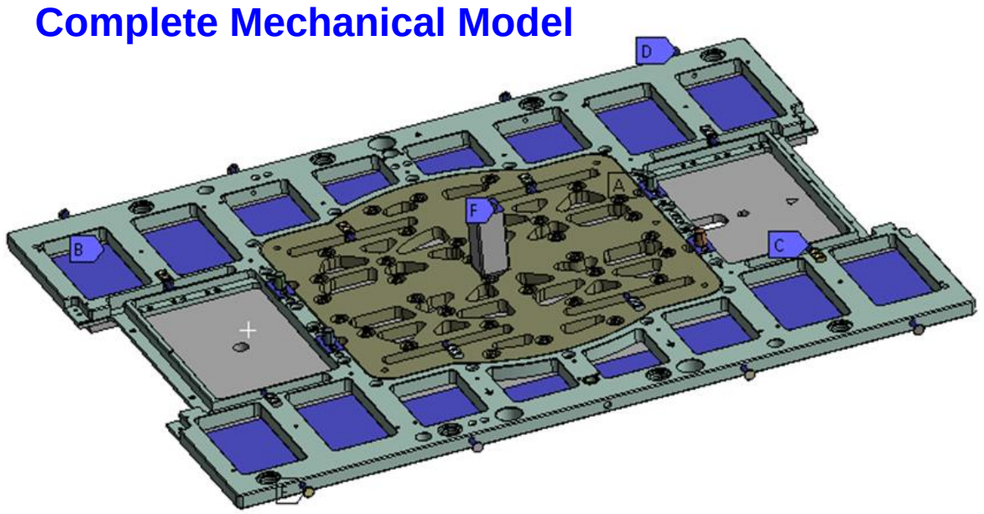
Thermal FEA to Control Deflection Due to Temperature

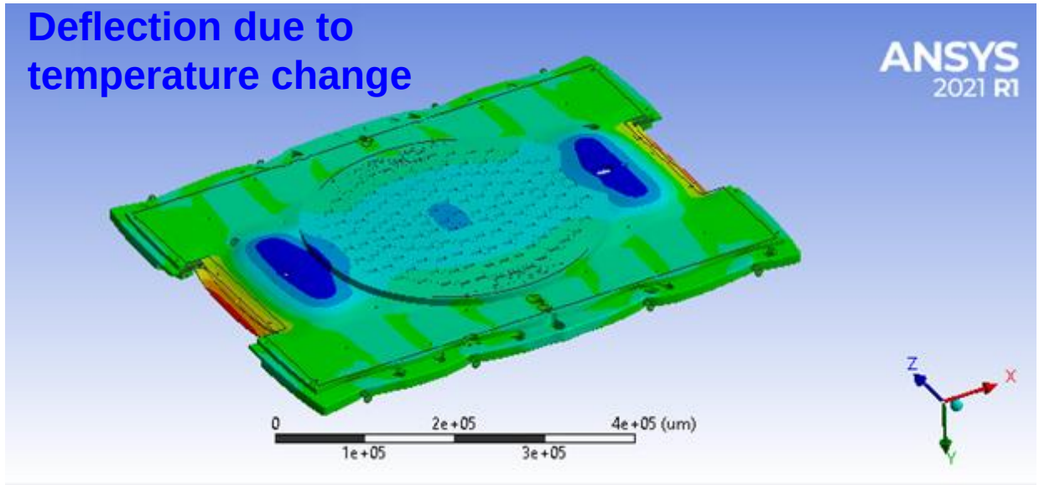
- Thermal gradients in probe card produce differential **expansion across probe card** components and can produce probe card bow



- Different Thermal FEA Simulations were needed to develop this solution and improve the PC performance by optimizing both:
  - Temperature Profile
  - Deflection due to temperature change on a full stack up PC

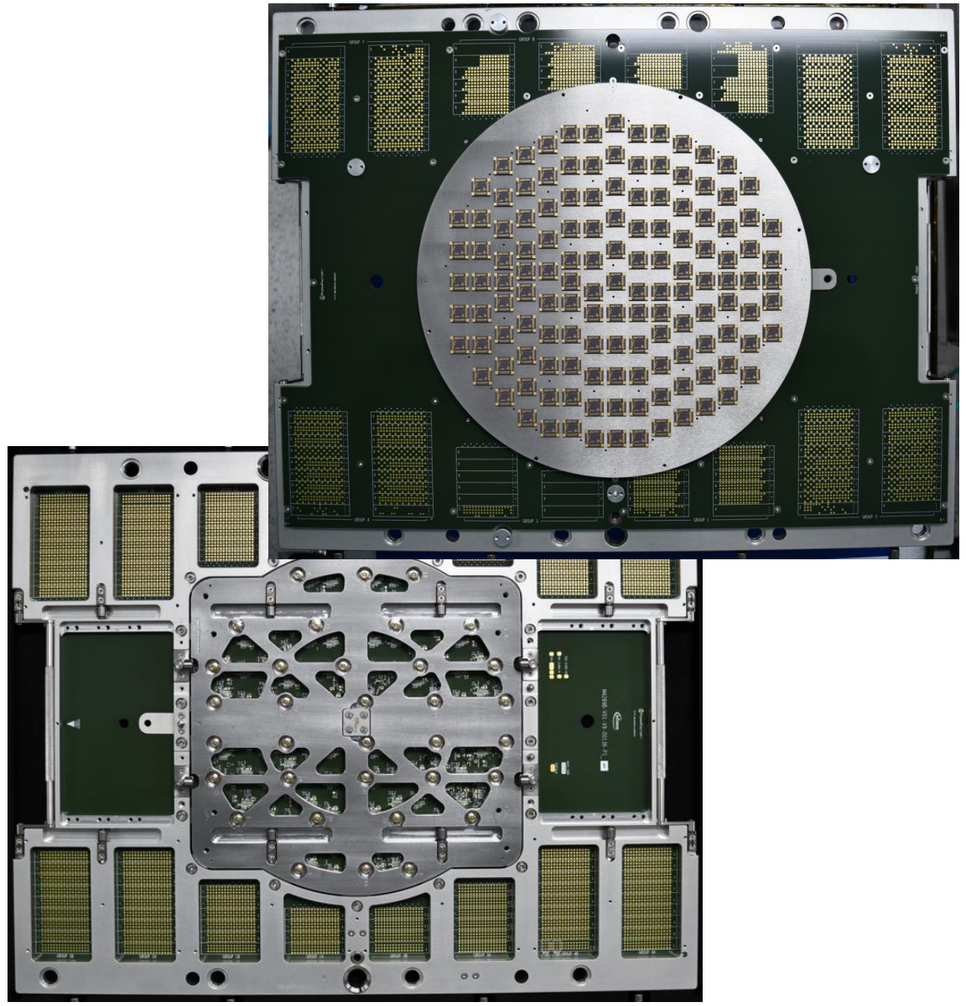






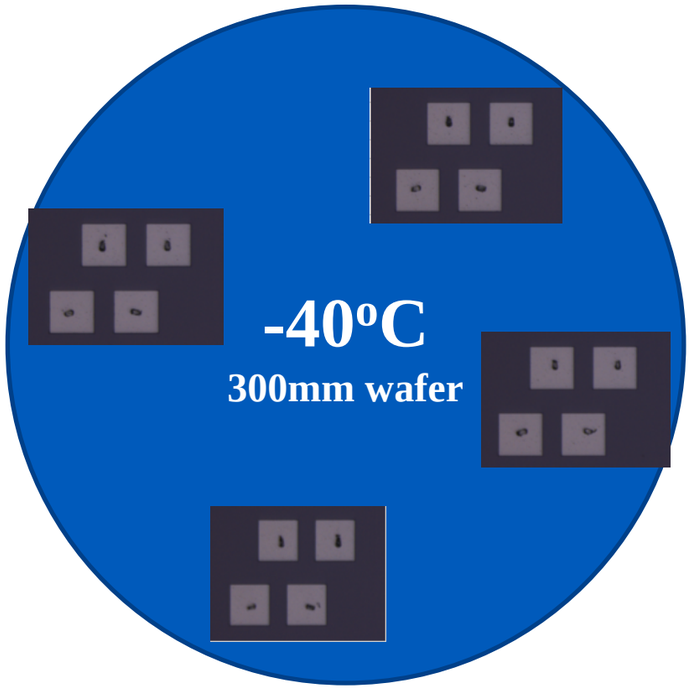
Validation Device Parameters

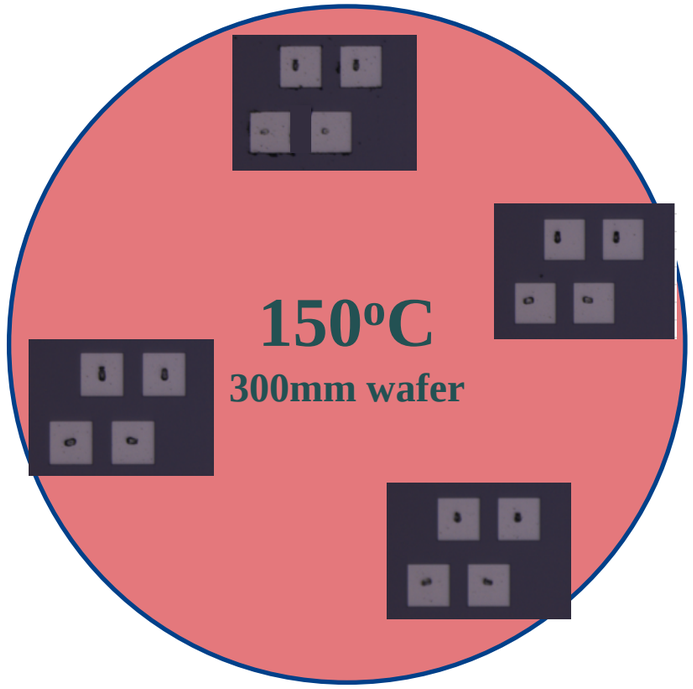
Test and Probe Card Parameters	
Total Probe Counts	> 20k
Minimum Wafer Pad Pitch	< 100um
Minimum Pad size	75um x 70um
Test Temperature Range	LT:-40°C & HT:150°C
Tester	Advantest V93K DD
Probe Technology	T11.2P
Max Sites available on tester	136
Parallelism	136
TD achieved	6
TDE	**93%**



TrueScaleMatrix Scrub Mark Capability

- Scrub mark results across full wafer array
  - Pad size: 70um x 75um
  - Scrub mark data collected on 300mm wafer at -40°C and 150°C
  - Ave. scrub mark size: 18um x 10um



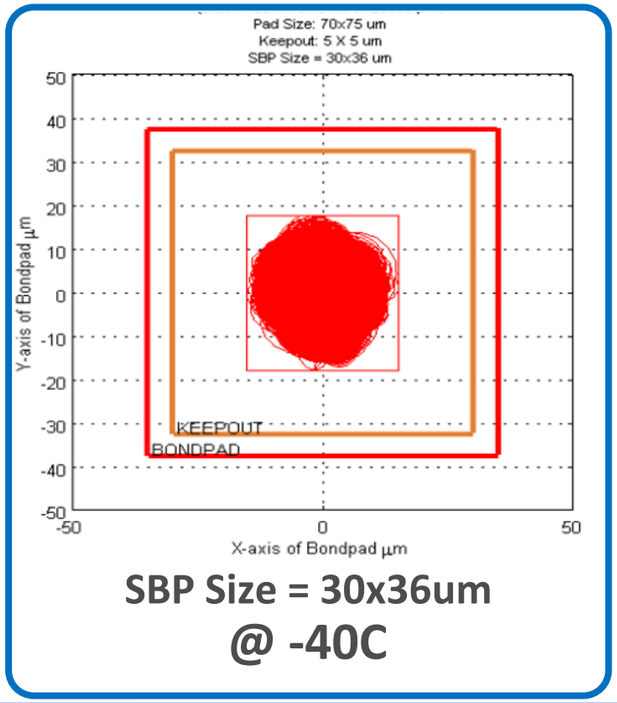


The location of scrub marks at the edge of wafer demonstrates the excellent thermal mechanical performance

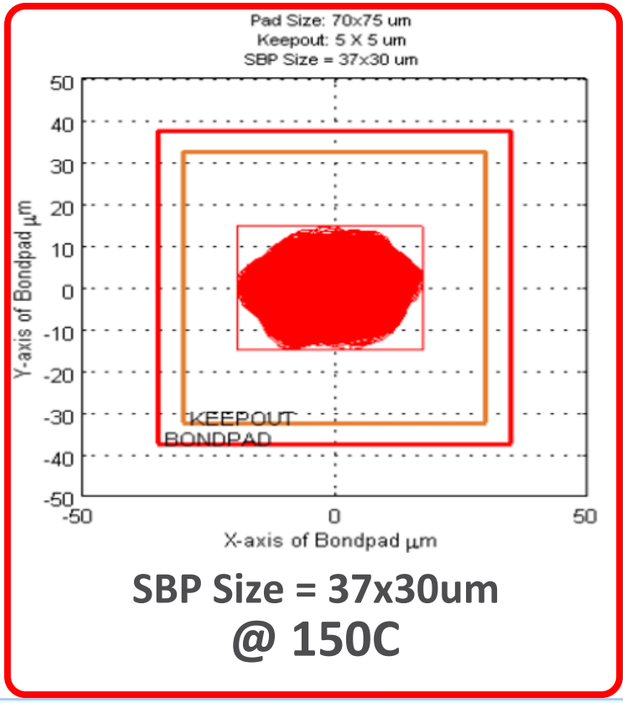
Super Bond Pad Capability at Full Temp Range

- Super Bond Pad (SBP):
  - Consolidation of scrub marks superimposed on top of each other to establish a single virtual pad representing all scrub marks
  - SBP calculation removes systematic errors not associated with the probe card capability

- Parallelism: x136
- Array size : Full Wafer
- Pad size: 70um x 75um
- Keep out: 5um
- 100% of scrubs in pad area meeting the keep out spec



SBP Size = 30x36um
@ -40C

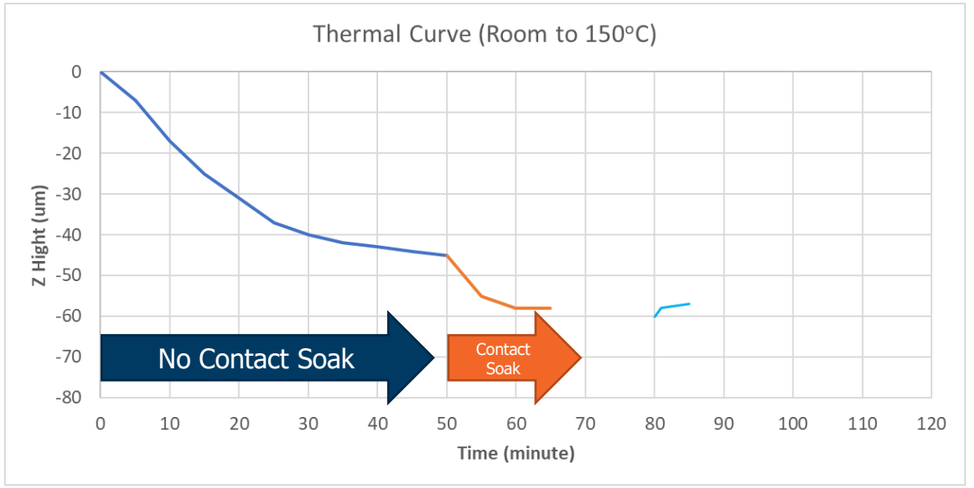


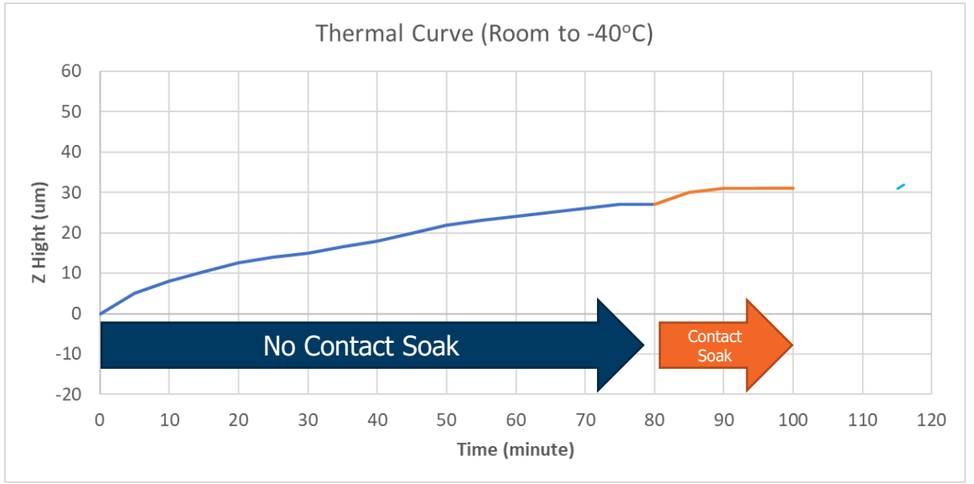
SBP Size = 37x30um
@ 150C

Demonstrated SBP performance <37um per side through entire temperature range

TrueScaleMatrix Thermal Characterization

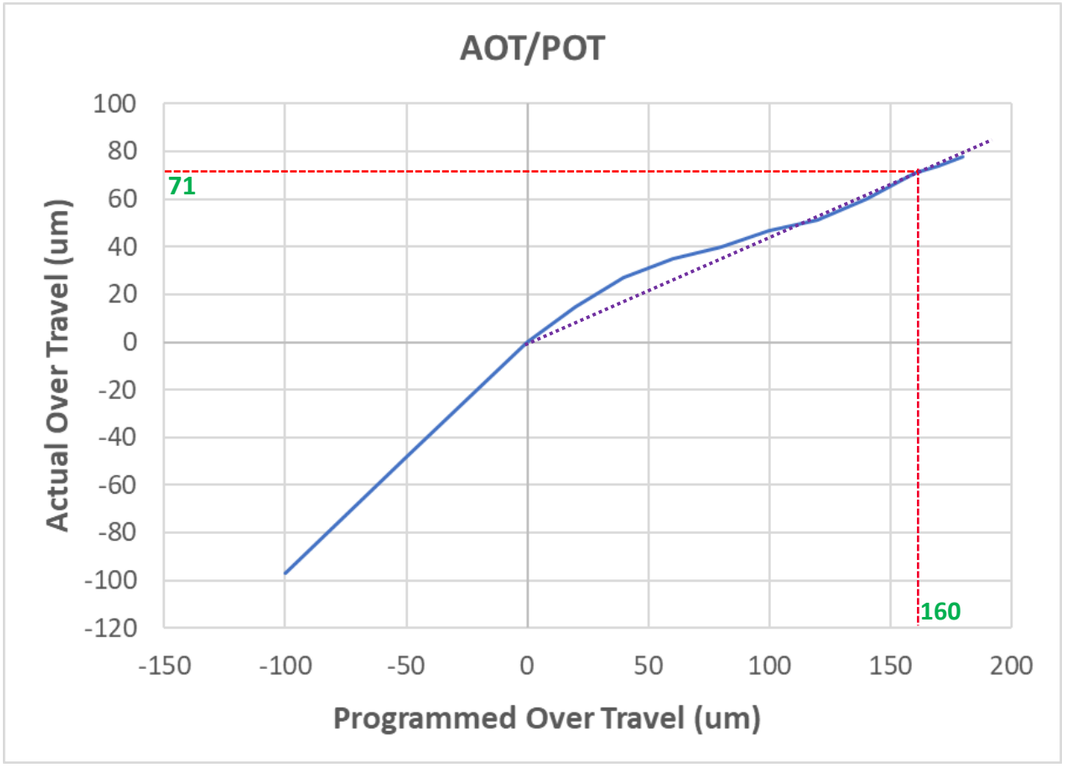
- Experiment for Room to 150ºC:
  - Measuring the change of height over time:
    - Full Wafer TSM with 20k probes
    - Prober preheated overnight before loading PC
    - Non-contact soak at -500um
      - 50 minutes
    - Contact soak to achieve final soak condition
      - 15 minutes and achieves thermal stability
  - Results:
    - ✓ Only 58um Z-height movement after complete soak
    - ✓ 2 um Z movement after chuck away from card for 1 min.
- Experiment for Room to -40ºC:
  - Measuring the change of height over time:
    - Full Wafer TSM with 20k probes
    - Non-contact soak at -500um for
      - 80 minutes
    - Contact soak to achieve final soak condition
      - 20 minutes and achieves thermal stability
- **Results:**
  - ✓ Only 31um Z-height movement after complete soak
  - ✓ 1 um Z movement after chuck away from card for 1 min.





TrueScale Matrix AOT/POT Experiment

- Objective:
  - Measuring the actual overtravel based on the applied programmed overtravel
  - Typically see AOP/POT deviate from 1 as pin count and parallelism increase
- Experiment:
  - Field Size: Full Wafer
  - Probe Count: ~20K
  - Tester: Advantest V93K DD
  - Prober: TSK Accretech UF3000 EX-e
- Results:
  - At recommended AOT of 70um the POT was measured 160um.
  - AOT/POT of around 44%

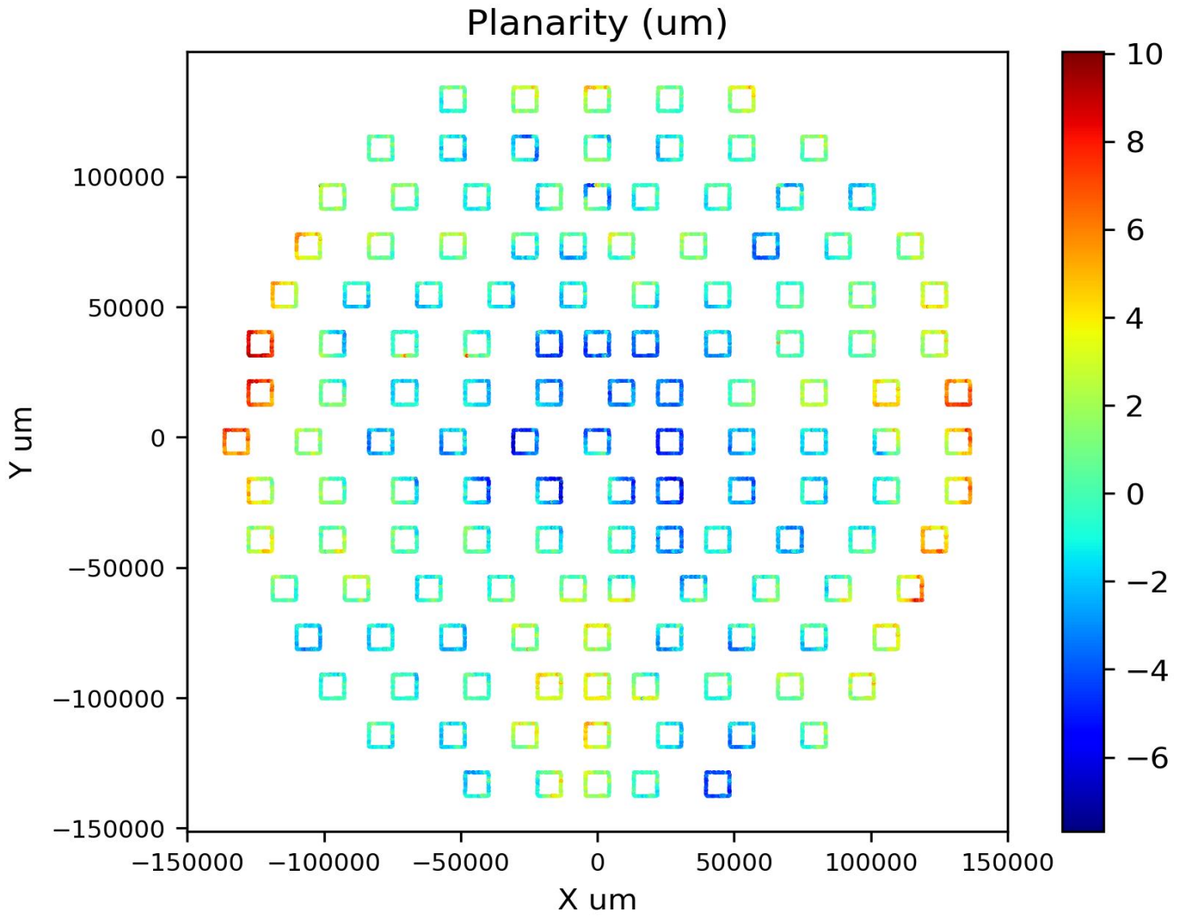


Demonstrated linear AOT/POT ratio around recommended actual overtravel

TrueScale Matrix Planarity Performance

- Measured outgoing Optical Planarity at FFI:
  - Typical performance of <20um on entire array

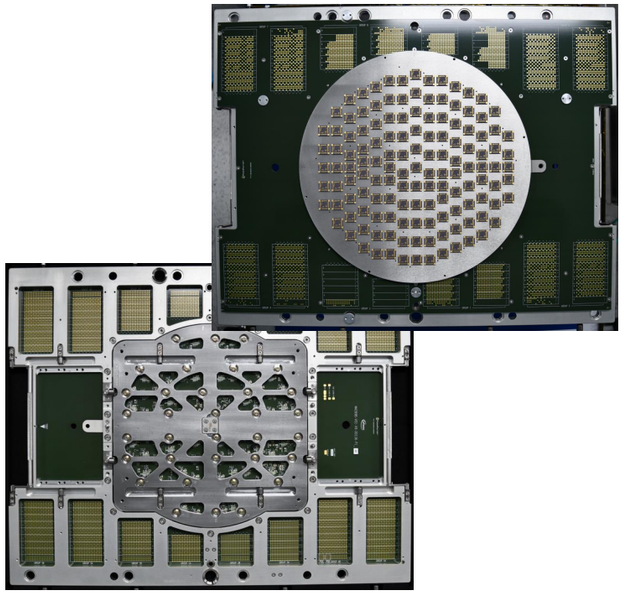
Planarity	Min.	Max.
17.8 um	-7.7um	10.1um

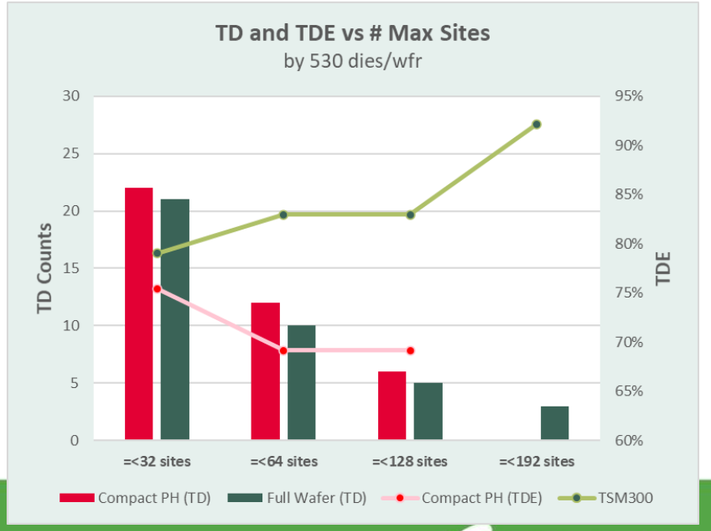


TSM provides excellent planarity of <20um across the full 300mm array

Summary

- Strong automotive IC market growth requiring not only lower test cost but also higher wafer throughput.
- Full wafer contactor solutions enables increased throughput and lowers cost of test compared to compact PH option
  - Increase parallelism to reduce TD count
  - Improve TD efficiency to optimize utilization of tester resources
- FormFactor has a full wafer contact solution for wafer test on V93K Direct-Dock tester
- The TrueScale Matrix 300mm full wafer contactor has been fully qualified for high parallelism automotive device probing





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