



# SWTEST

PROBE TODAY, FOR TOMORROW

2024 CONFERENCE

## Optical edge coupling method for fully automated PIC wafer-level testing



Dan Rishavy, Joe Frankel, Quan Yuan,  
Simon Reissmann

Anna Peczek, Christian Mai, Georg Winzer,  
Lars Zimmermann

# Overview

- Introduction
- Probing features
- Component of the system
- Requirements and DUT
- Wafer-level results
- Summary

## Innovations for High Performance Microelectronics



Frankfurt (Oder)

Institute for R&D & Prototyping



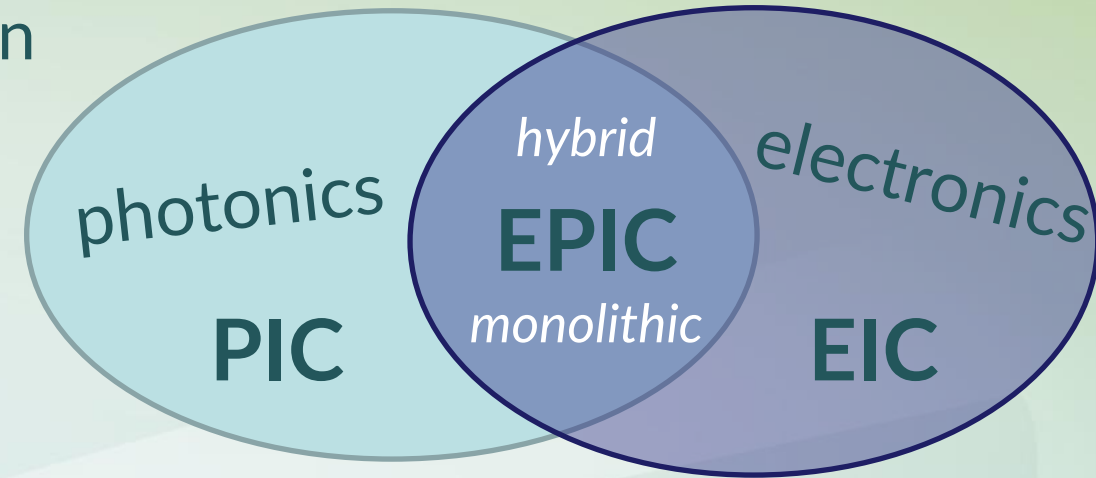
- RF SiGe BiCMOS Technology
- 0.25  $\mu\text{m}$  and 0.13  $\mu\text{m}$  CMOS
- 200 mm wafers
- 100 WSW
- Silicon Photonic MPW (SiPh and BiCMOS)

# Silicon Photonics

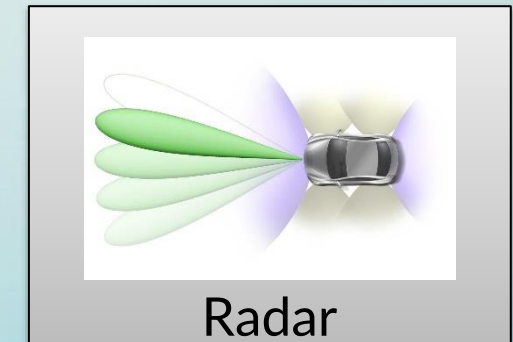
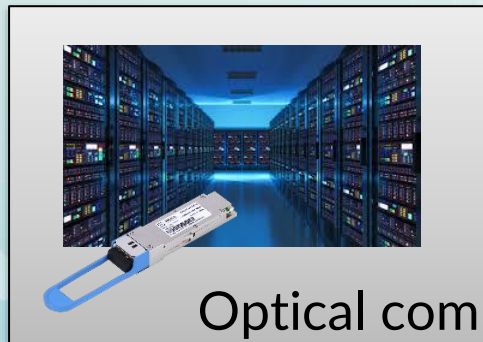
- Photonics building blocks realized in silicon technology:

- Waveguides
- Grating/edge couplers
- Phase shifters
- Photodiodes

can be combined with electronics.



- Application space



# SILICON PHOTONICS

## fits to microelectronics value chain



Electronic design  
automation EDA

**cadence**<sup>®</sup>



Is optical probing already established on the same level as electrical probing?



# Electrical probing

## State-of-the-art:

- Automated probing on wafer
- Vision probe recognition
- High repeatability
- High throughput

**We expect the same from optical probing !**

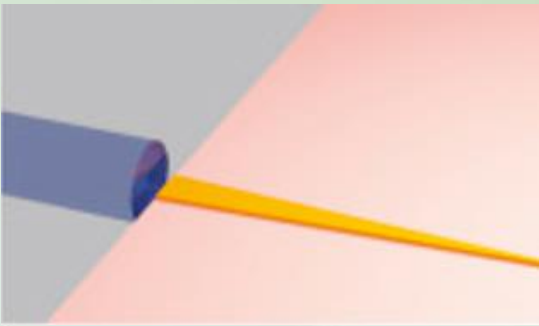
# Optical vs. electrical probing

- In contrast to electrical probing exact optical probe placement matters, also in Z direction
- Prober XY accuracy:  $2 \mu\text{m}$  ( $1\sigma$ )
- Chuck planarity:  $\pm 5 \mu\text{m}$

## Required:

- Position accuracy in sub micron range
  - non contact optical power optimization
- Height control of the fiber
- Reasonable time for the alignment

# On-wafer optical coupling interfaces



	Grating coupler	Edge coupler
Test methodology	vertical	horizontal / edge
Fabrication effort	without extra	with extra
Footprint	small	medium
Equipment (Cost)	low	high
Coupling loss	> 3dB	<2 dB
Polarization dependance	high	low
Bandwidth	<40 nm	> 100 nm
On- wafer testing	available	Now available

*drawbacks*

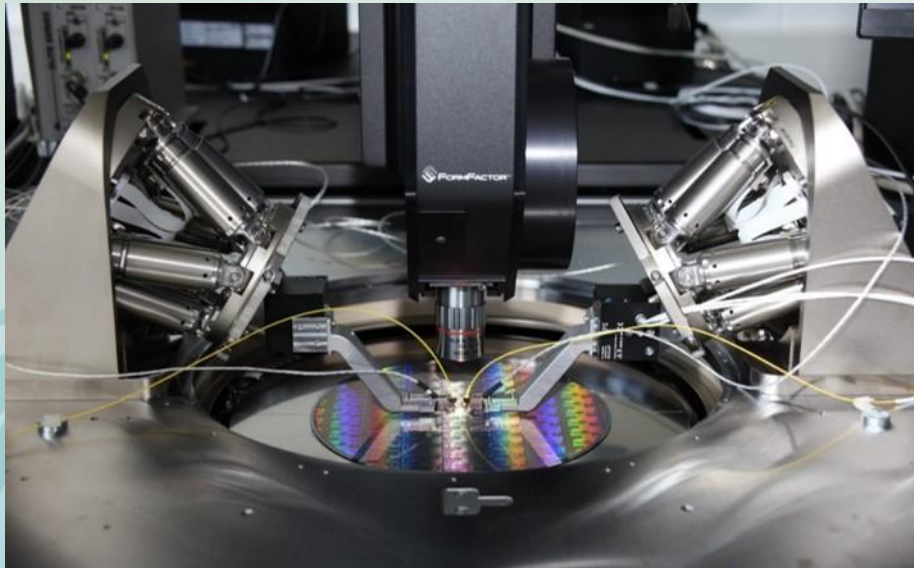
*benefits*

Source of pictures: <https://www.sciencedirect.com/science/article/abs/pii/B9780128133538000087>

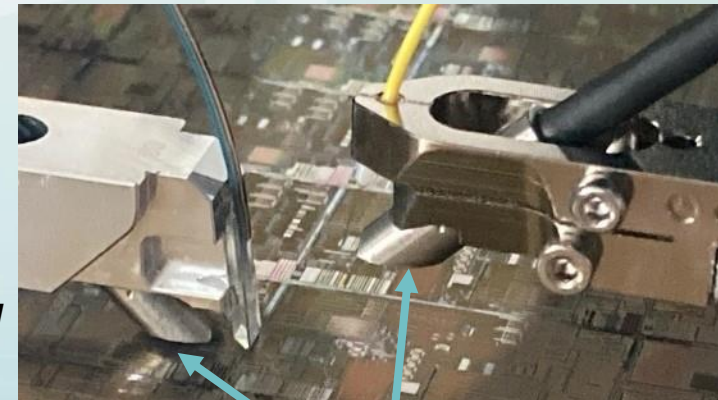


# Equipment for on-wafer PIC characterisation

- 300 mm Probe Station FormFactor CM300xi with Loader
- 6-axis positioners with Nano Cubes (PI)



- Optical Probe



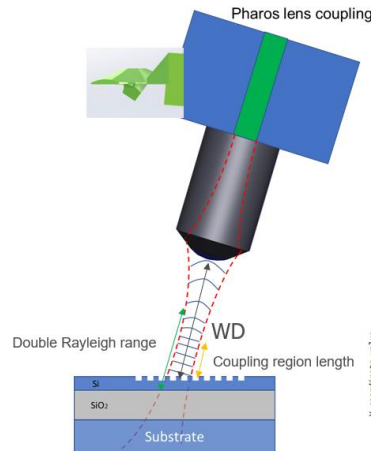
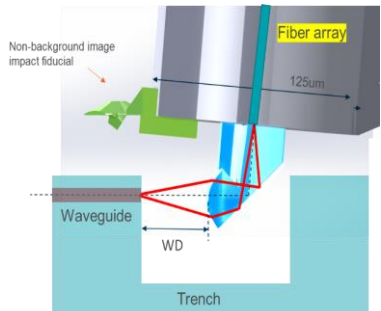
Pharos aLens  
for horizontal/ edge  
coupling

Cleaved Fiber  
for vertical  
coupling

CAP sensors

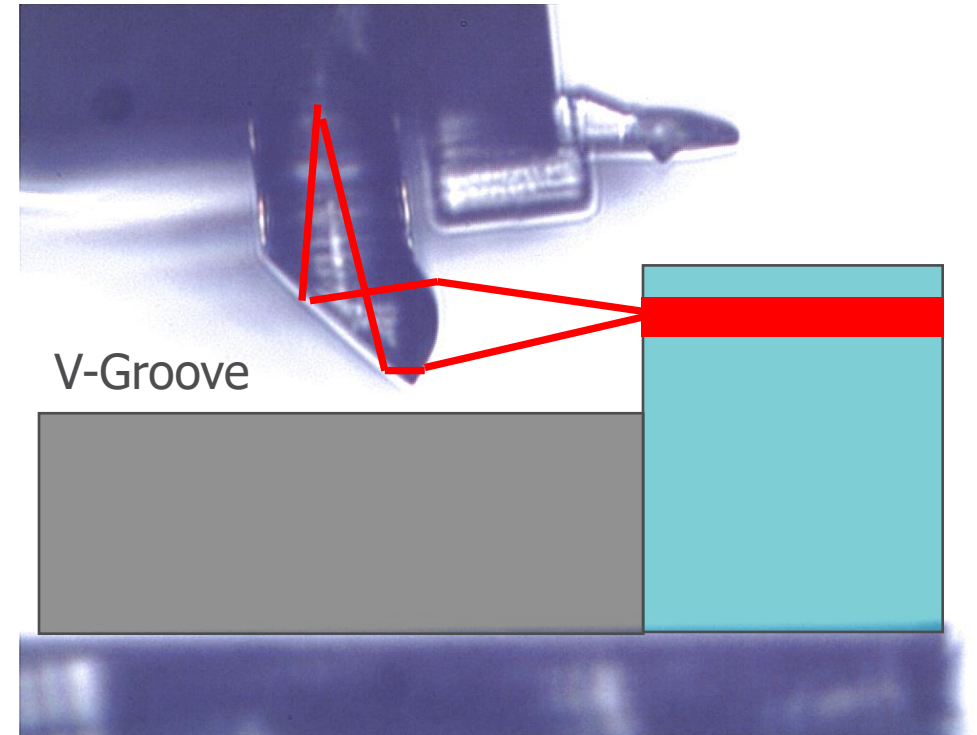
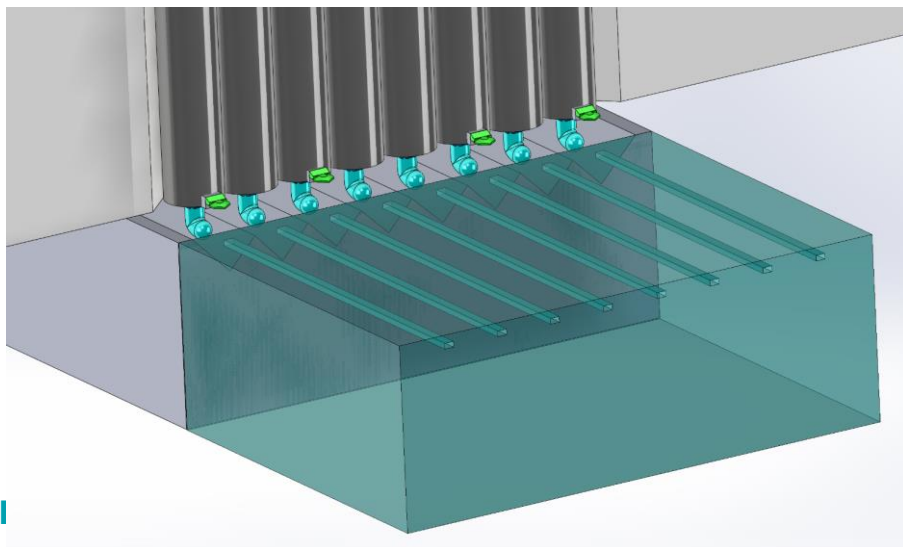
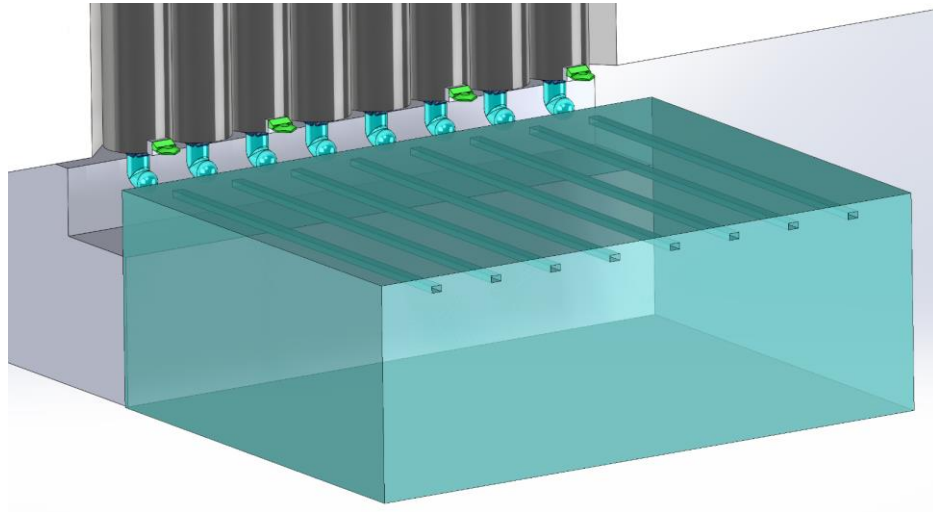
# Pharos Lens for Silicon Photonics Probing

**Pharos**<sup>TM</sup>  
Technology



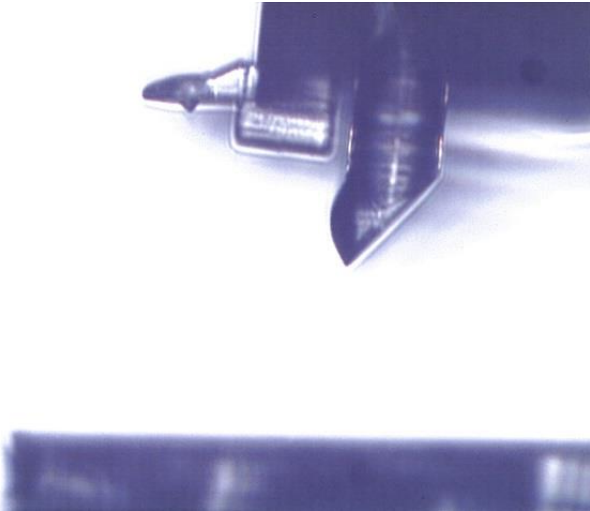
- Wafer level edge and vertical coupling designs
  - Short and long working distance designs
- High coupling efficiency
- High repeatability and stability
- Nearly collimated beam with Plane front wave at grating coupler taper
- Ultra long working distance(WD) possible – ex. up to >800µm
- Tolerant in Z (beam propagation direction) for vertical
  - i.e. large coupling range
- Mode field diameter and working distance

# Applicable for wafer level trench and v-groove

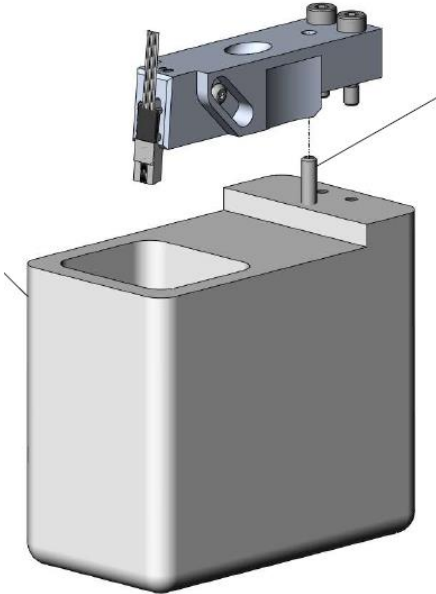
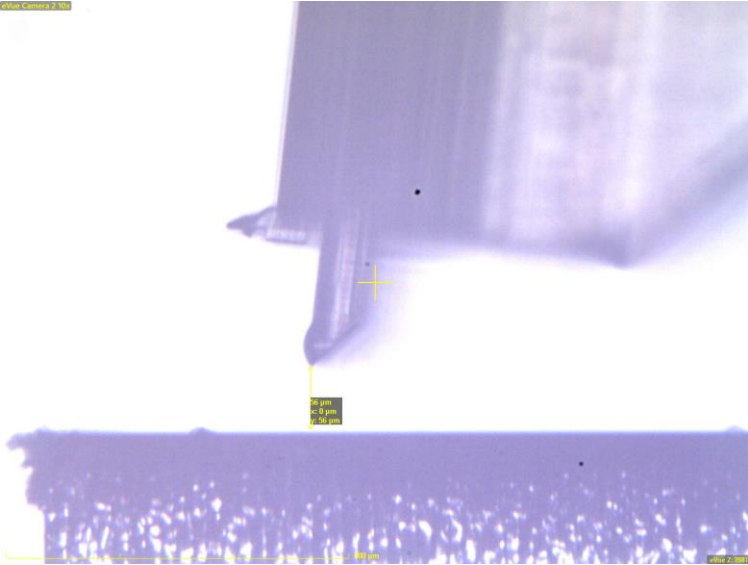


# Pharos Lenses for Grating and Edge Coupling

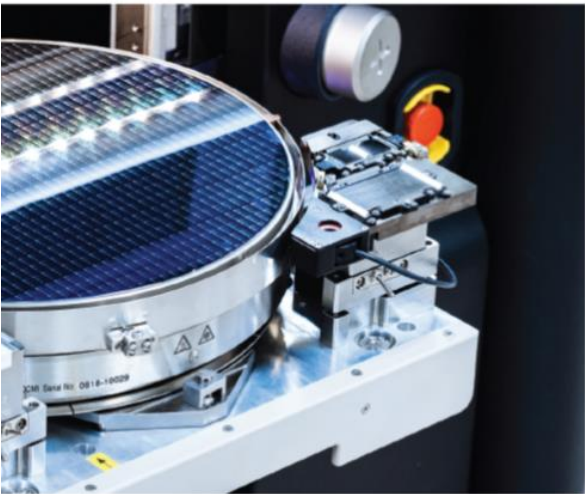
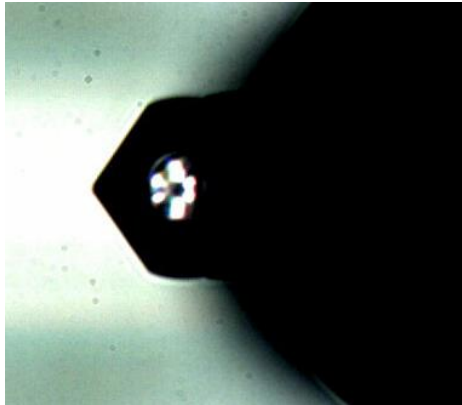
Short Edge Pharos lens (Trench)



Long Edge Pharos lens (V-groove)



Top View (Fiducial)

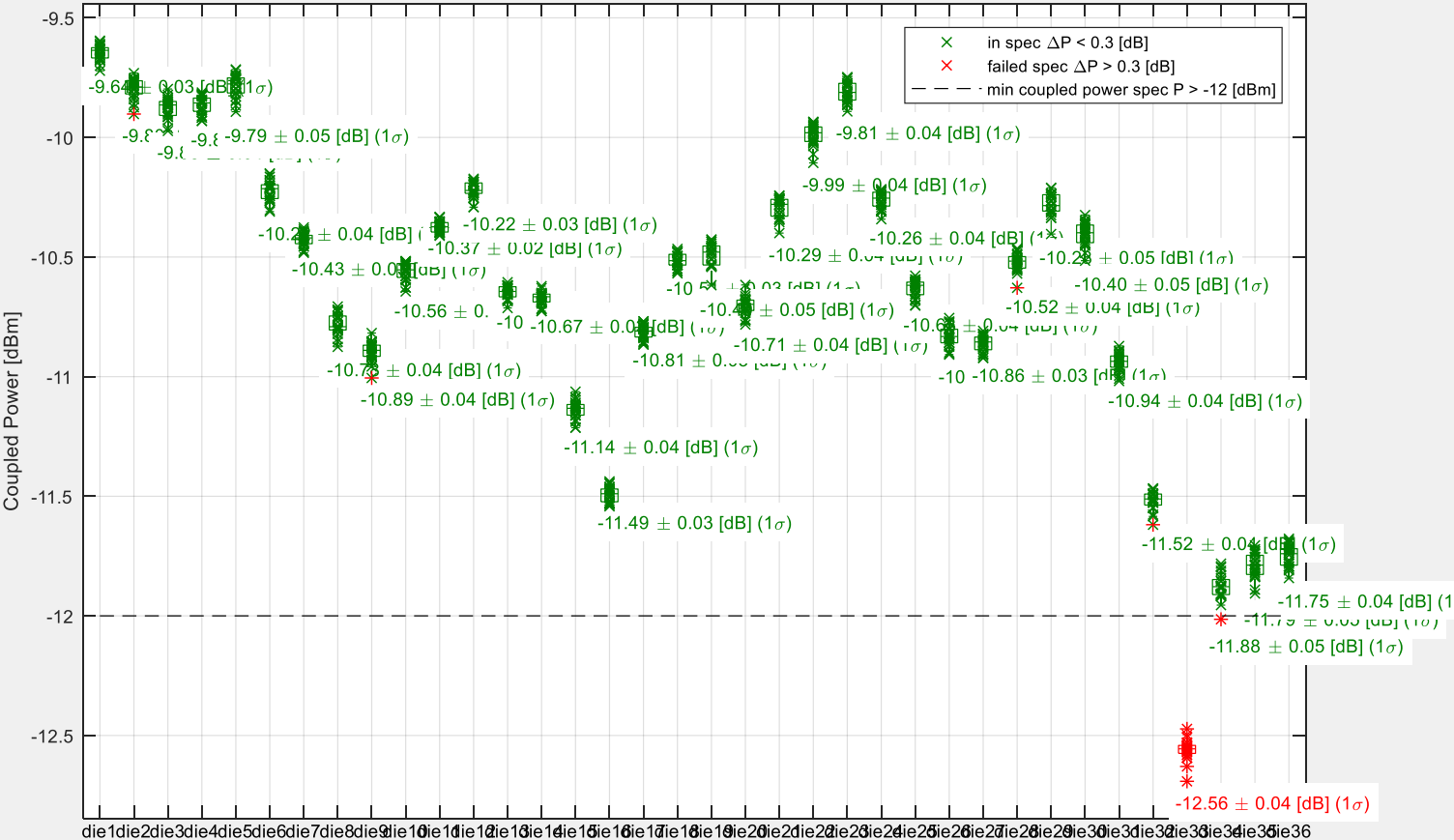


OptoVue Pro

# Coupled Power by Structure – LB1\_8

SiPh Verification Test Summary  
Single-Sided West

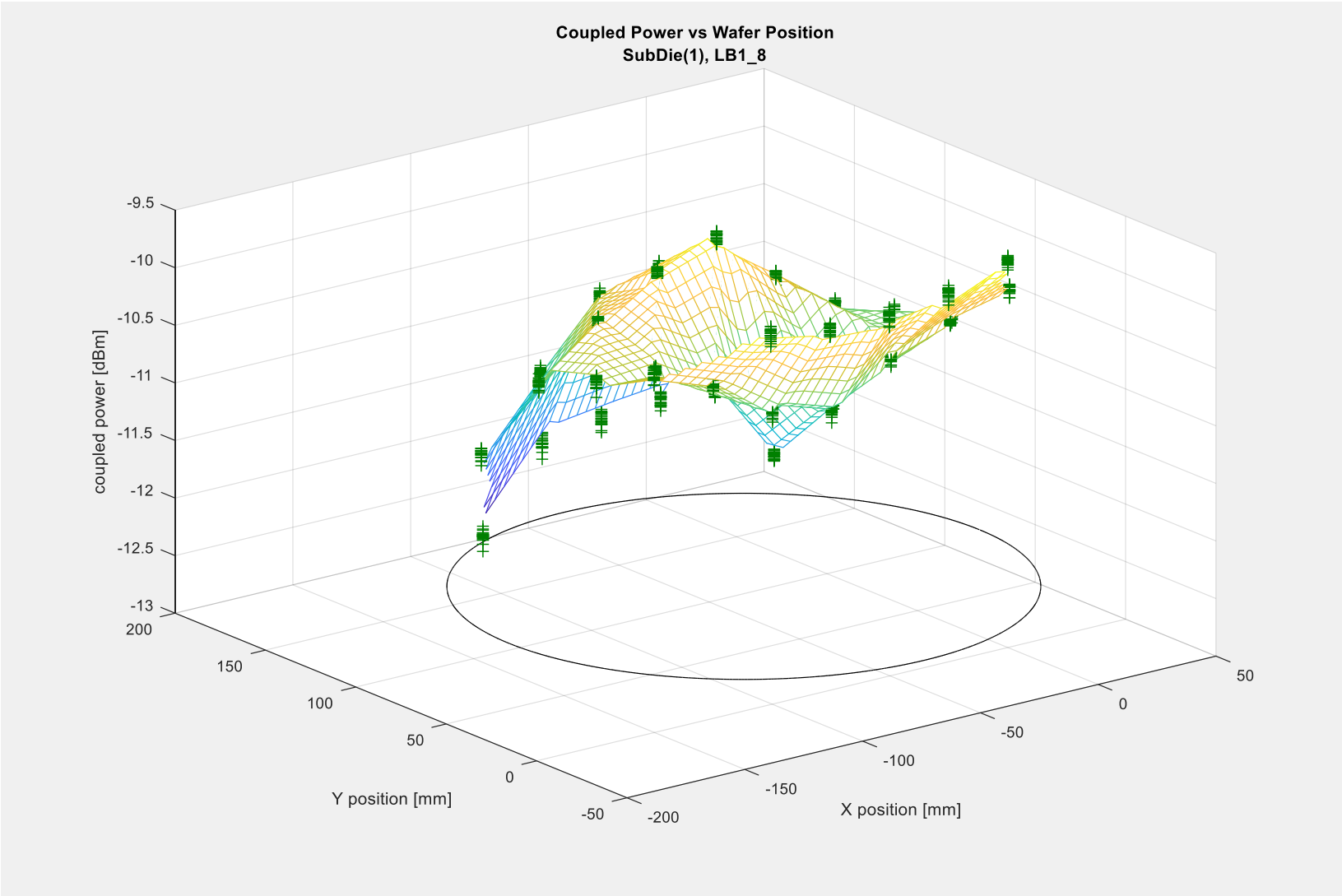
SubDie(1), LB1\_8, SN# 1836175, Jun 12 2021, 7:02 PM  
36 structures, 865 measurements,  $\sigma_{tot} = 0.04$  [dBm], result : FAIL



36 die  
1 subdie  
4 channels  
24 passes

# Coupled Power vs Wafer Position – LB1\_8

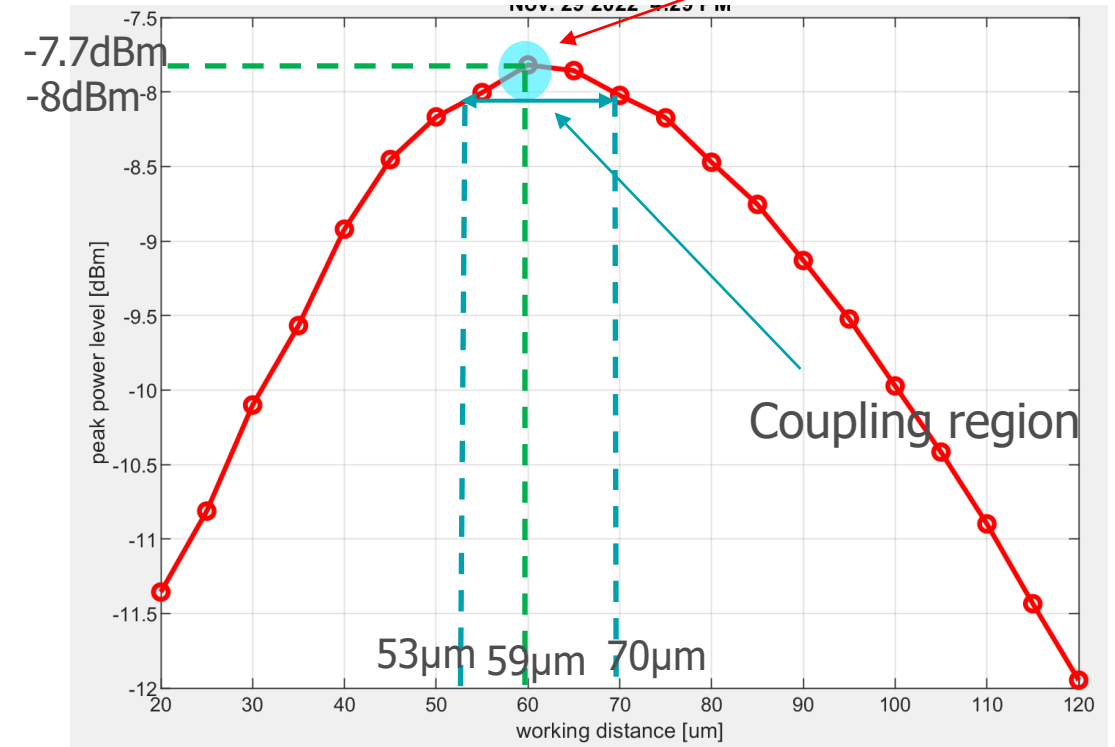
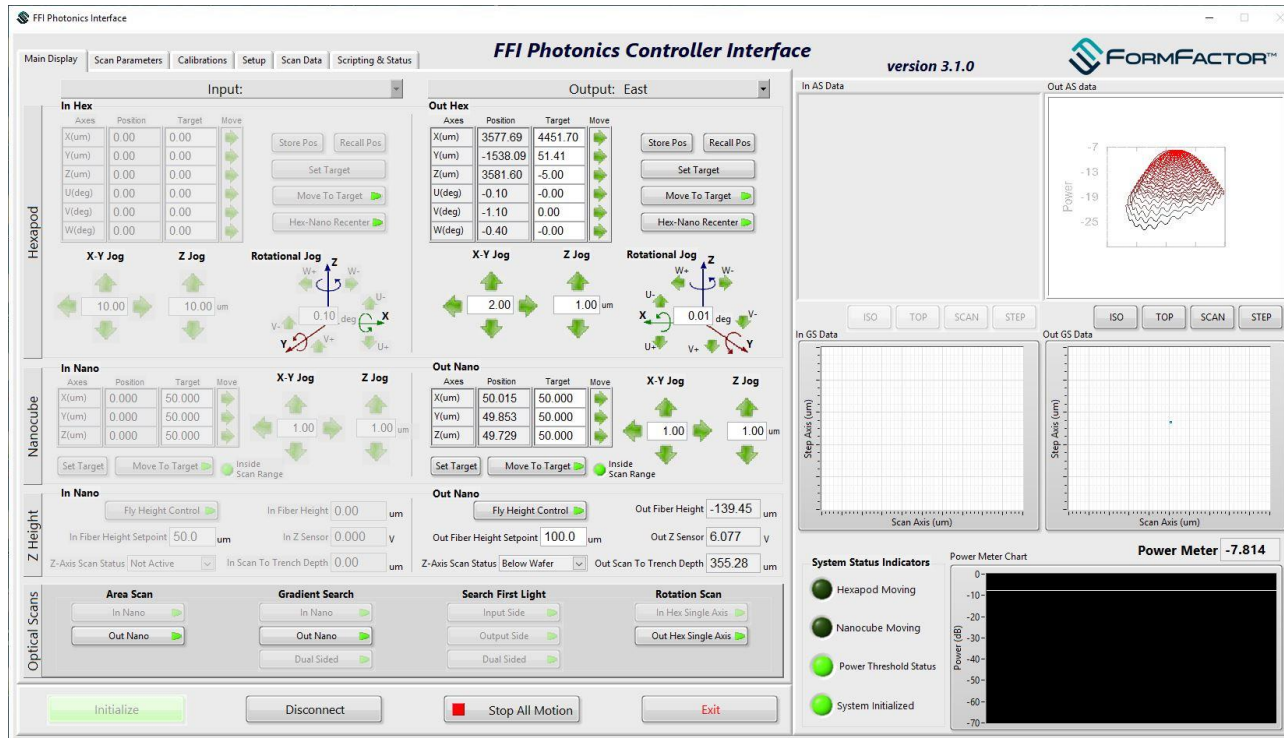
**36 die**  
**1 subdie**  
**4 channels**  
**24 passes**



# Scanning and 3D coupling result-Long Lens (MFD=6μm)

One scanning example

Max coupling at 59μm which agrees with simulation



Input power -2.2 dBm

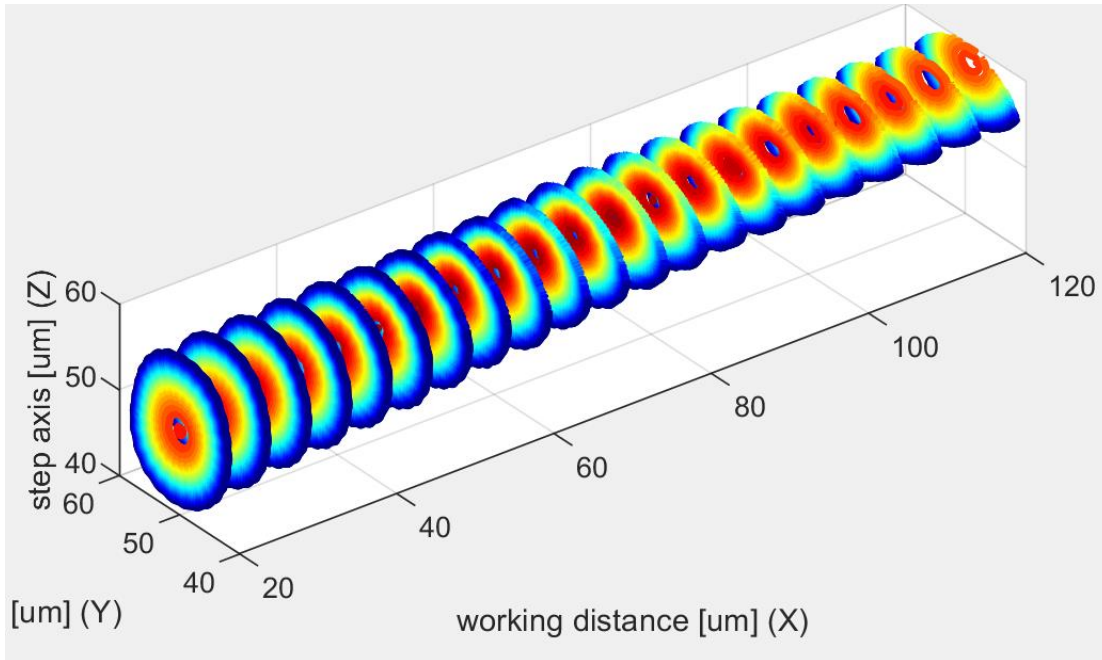
Power coupler loss  $(7.7-2.2)/2=2.75\text{dB/faucet}$

# 3D coupling indicate the waveguide beam direction in Edge coupling (6um) – V-Groove

Power coupling contour in 3D dimension (Color indicates power level)

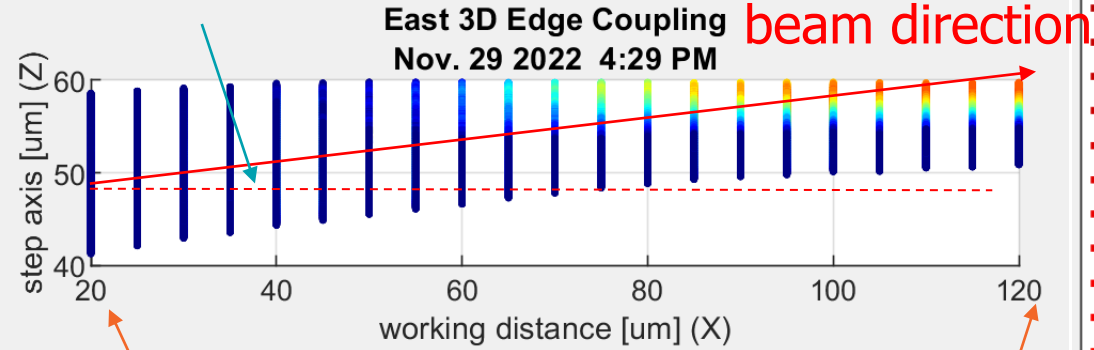
ISO view

20um Spiral Scans



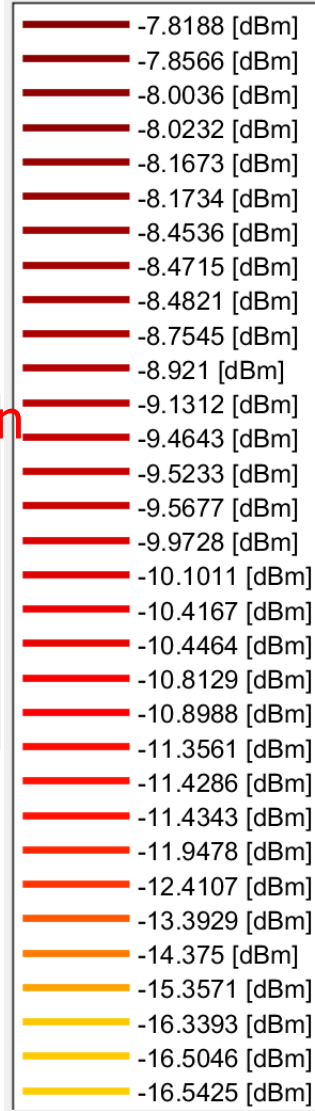
X-Z view

Angle  $\approx 6$  deg



20 um away from Waveguide

120 um away from Waveguide



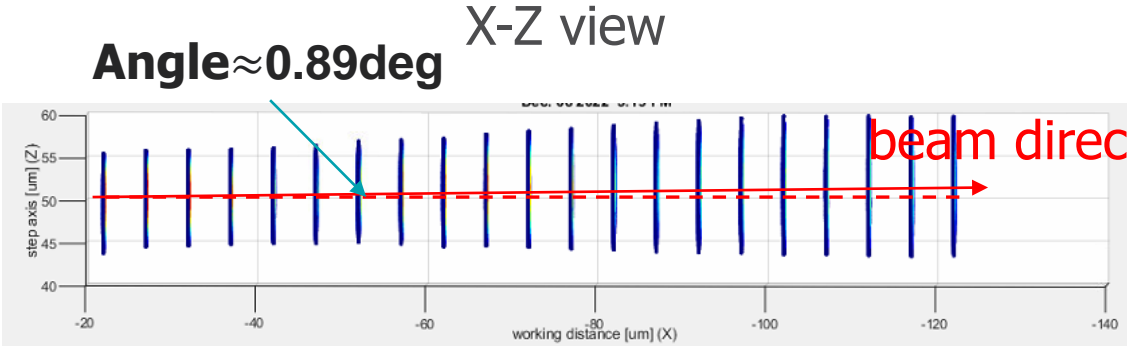
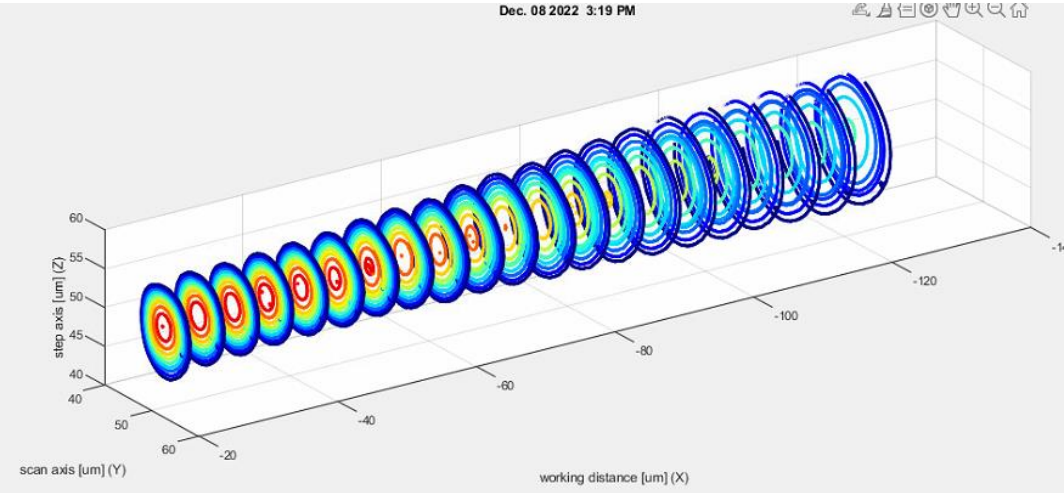


# 3D coupling indicate the waveguide beam direction in Edge coupling – Trench

Power coupling contour in 3D dimension (Color indicate power level)

ISO view

20um Spiral Scans

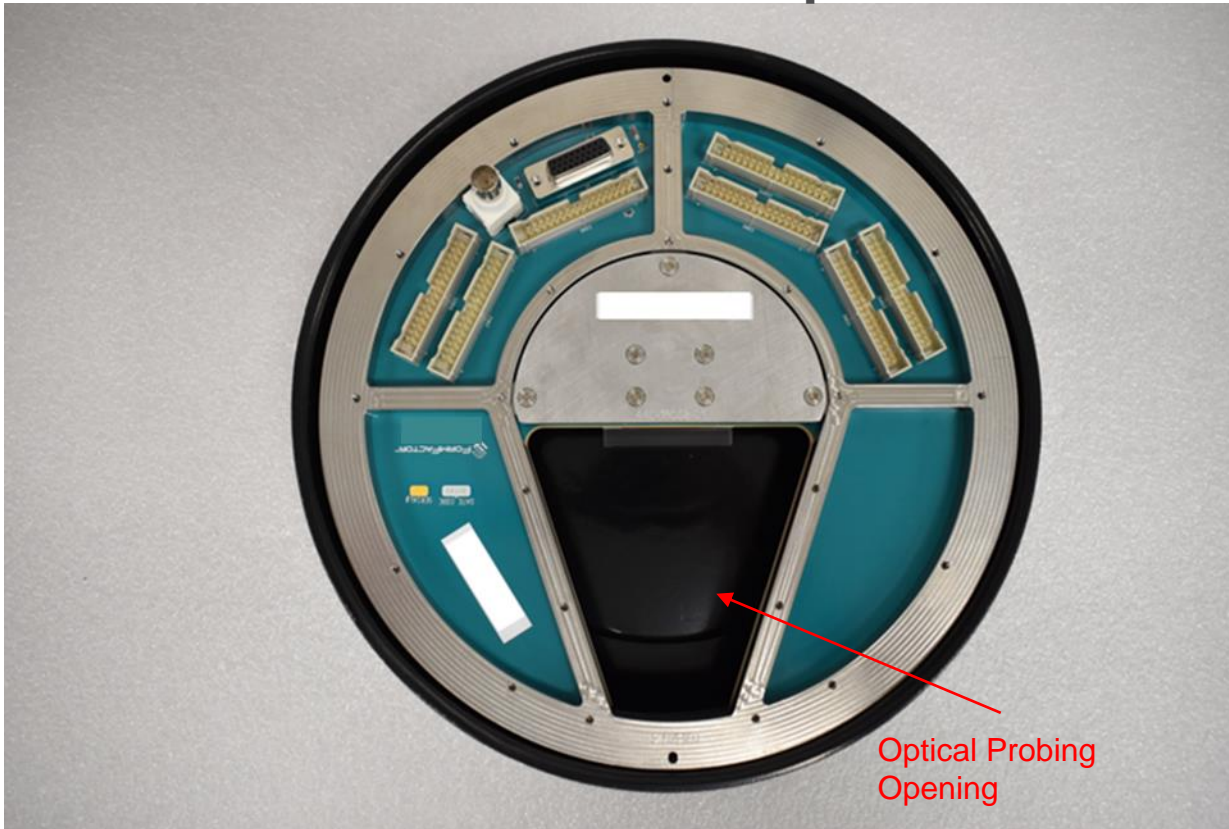


# Probe Card Integration

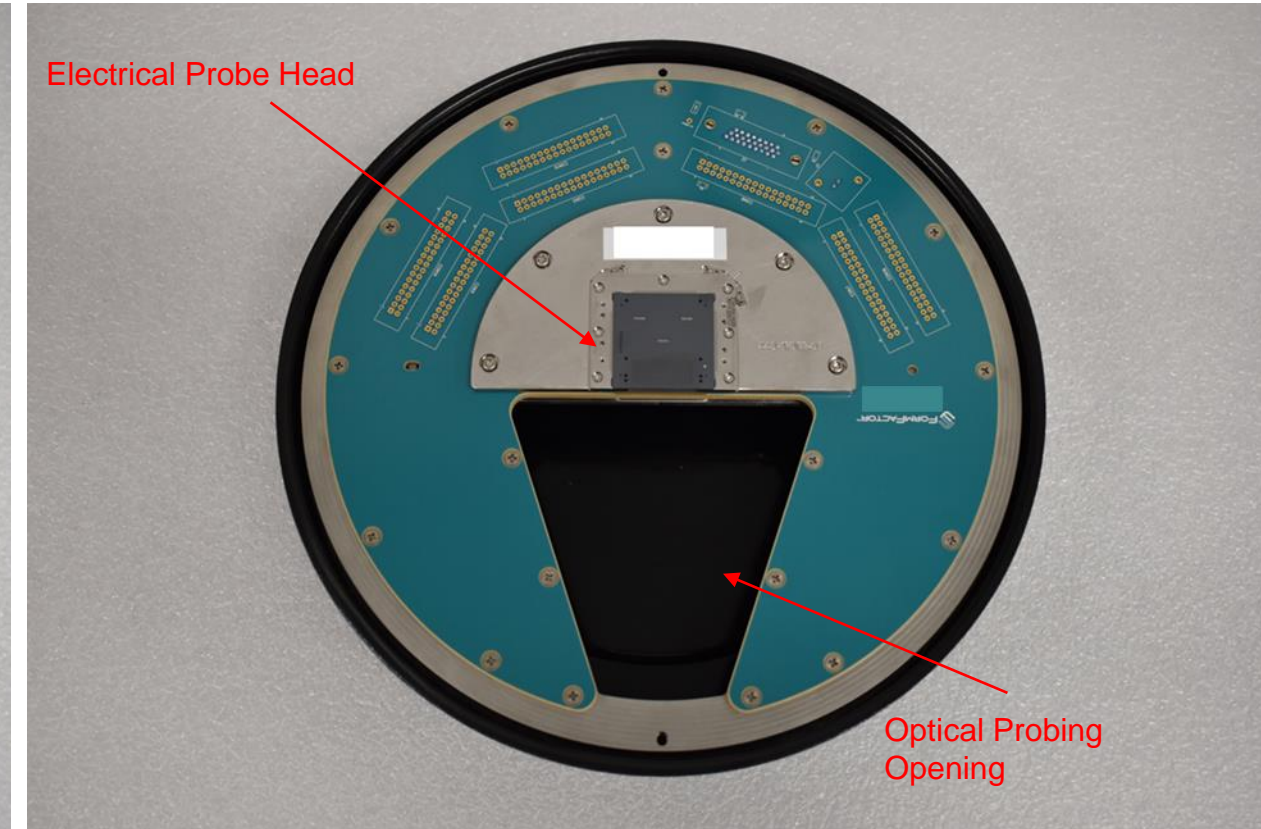


# FFI Apollo Probe technology adapted for SiPh probing

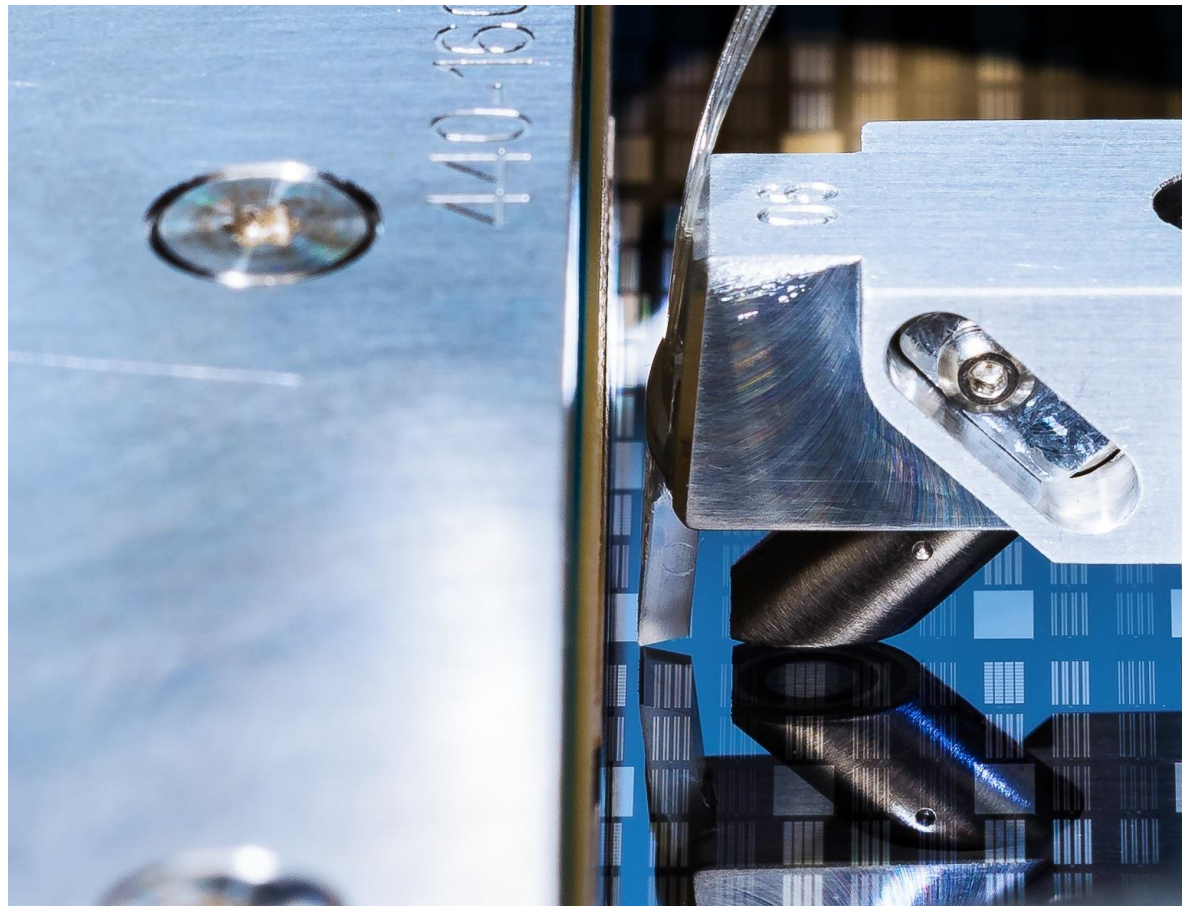
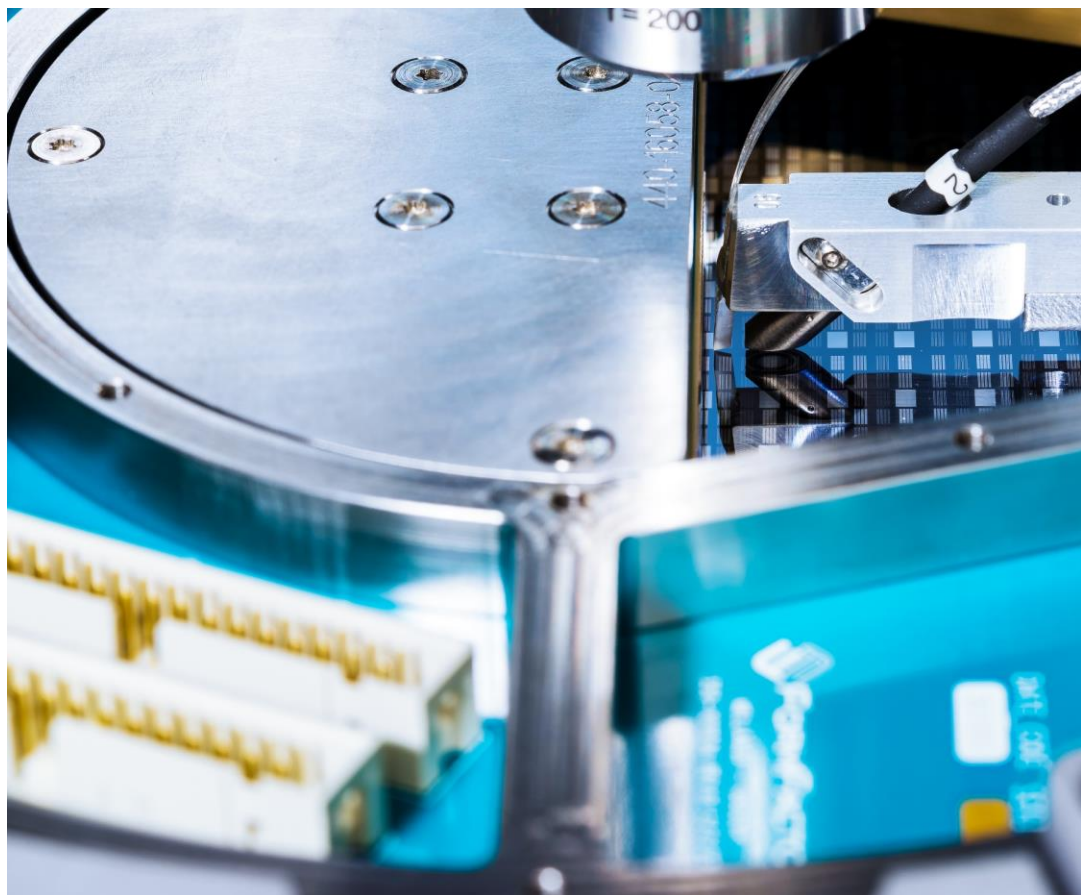
Probe Card Top View



Probe Card Bottom View

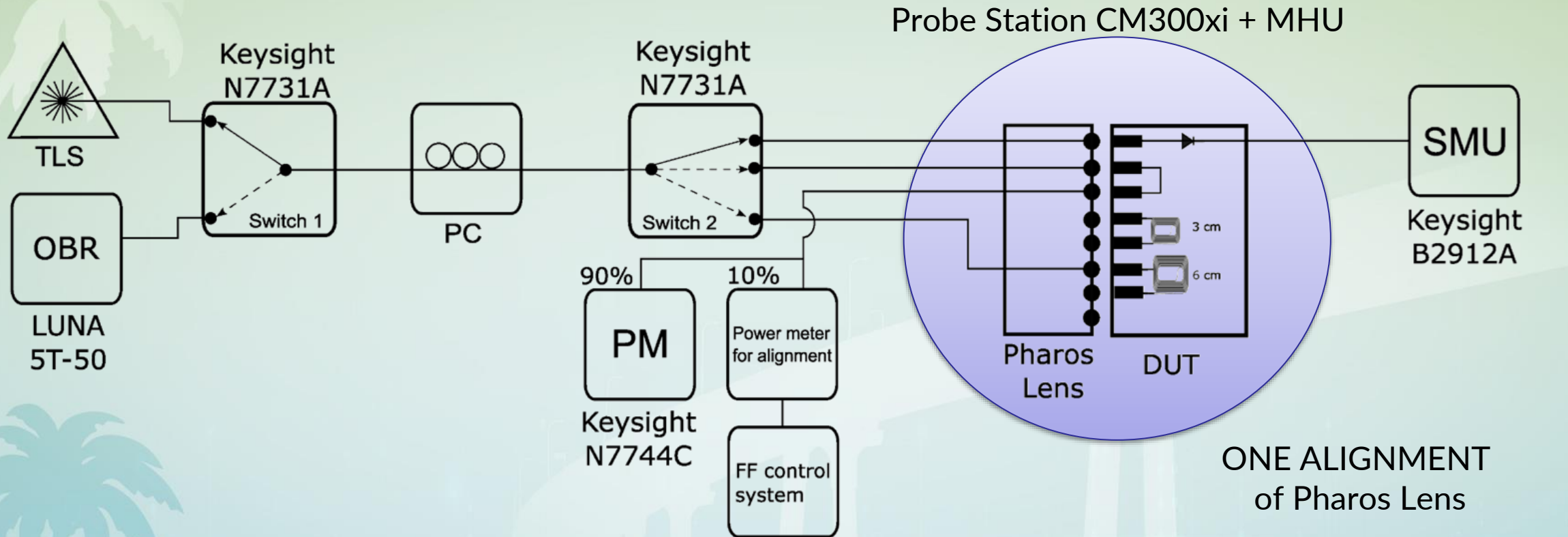


# Probe Card Integration with Edge Coupling Pharos



FFI Apollo and Pharos Probe Technology is currently being used for production testing of edge coupled wafer level V-groove Co-Packaged Optics devices

# Test setup at IHP

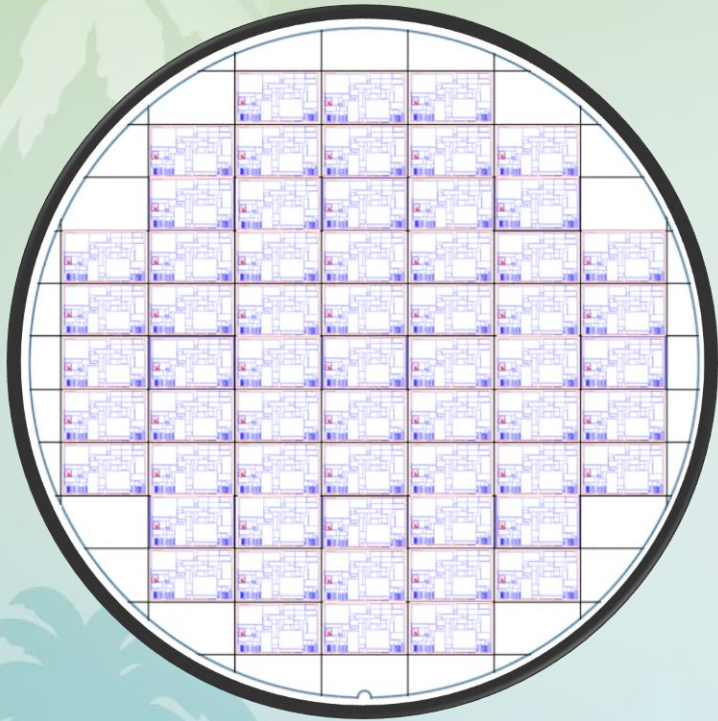


ONE ALIGNMENT  
of Pharos Lens



- Coupling loss
- Waveguide loss
- Photodiode responsivity

# Device under test



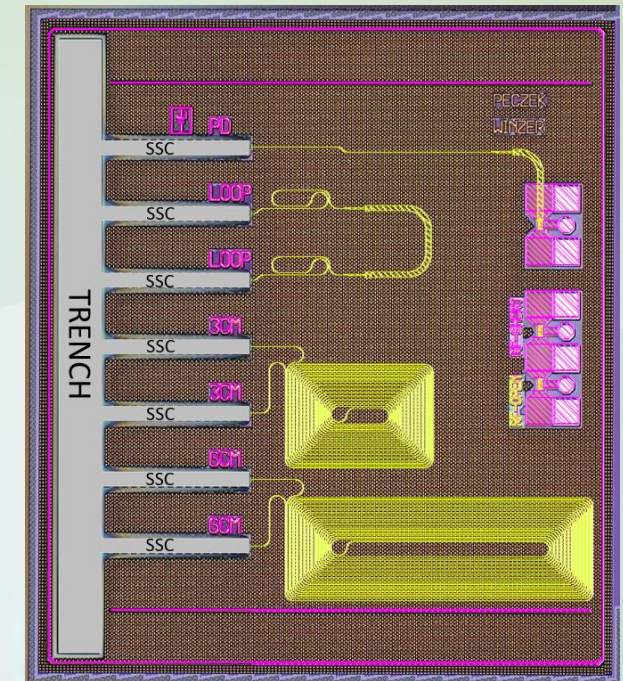
200 mm PIC wafer

Up to 61 dies

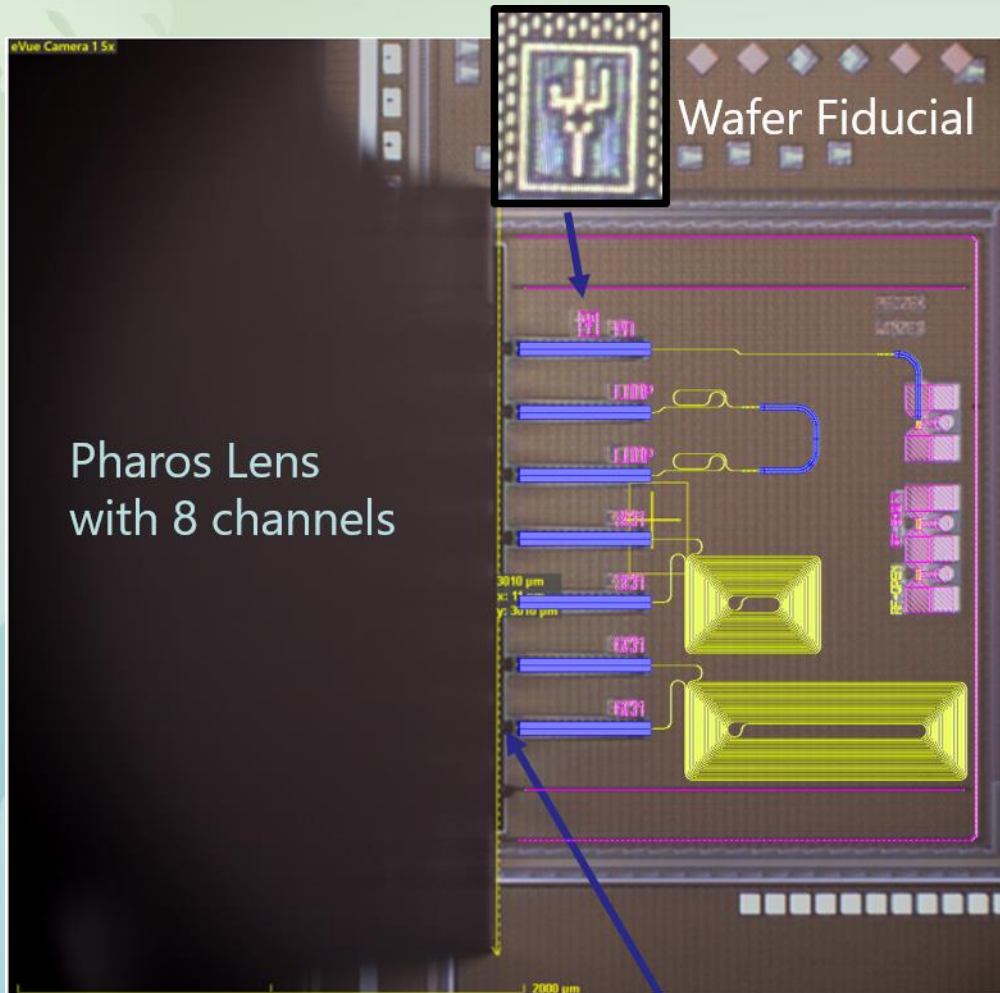
Test chip consist on:

- Ge photodiode
- Waveguide loop
- 3 cm long waveguide
- 6 cm long waveguide

Photograph of the test chip with overlapped layout



# Design and fabrication requirements



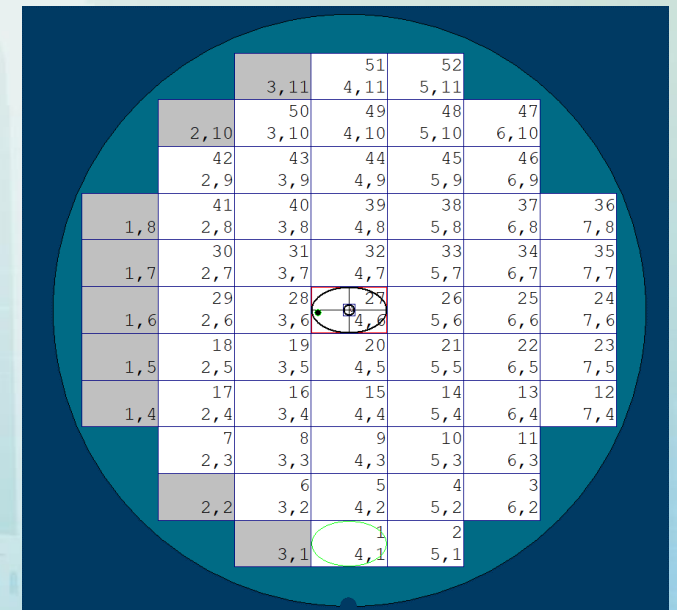
## Requirements:

- Trench width  $> 95 \mu\text{m}$
- Trench depth  $> 60 \mu\text{m}$
- Wafer fiducial present
- Pharos spot size range 2-10.2  $\mu\text{m}$

# Testing step by step

1. System Calibration → *Essential for accuracy and automation*
2. Trench quality control → *Important to not damage the Pharos Lens*
3. Selecting the test dies
4. Calibration of the optical path and measurement instruments
5. Preparation of the measurement project (IC-CAP Keysight)
6. Running the measurement sequence ...  
..... and waiting for the results.

Grey chips excluded from tests due to trench imperfections

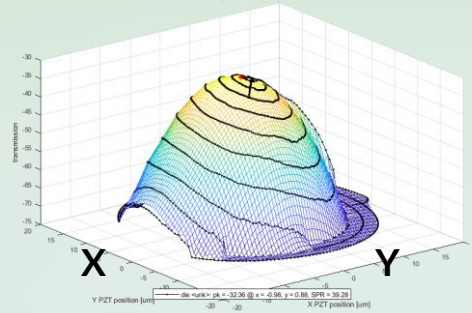




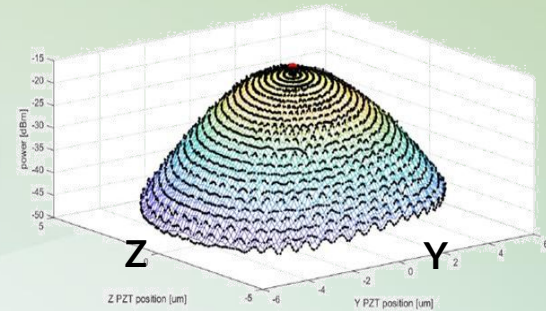
# Alignment

Fully automated, algorithm-based with user-defined parameters

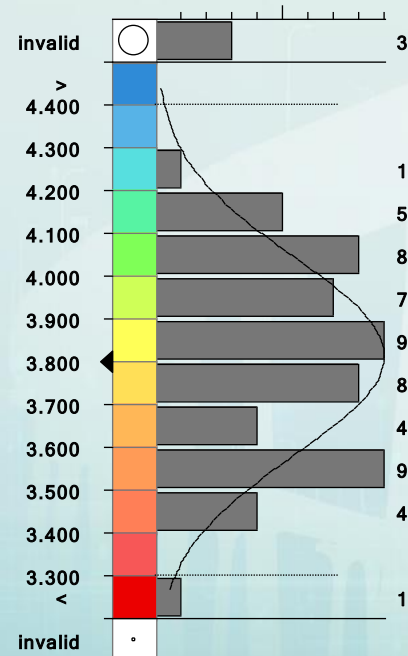
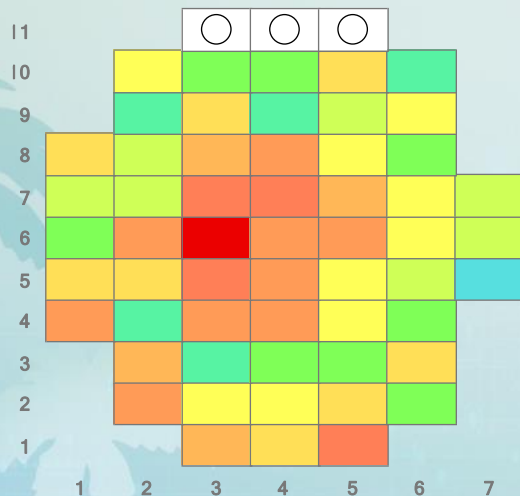
## Grating coupler



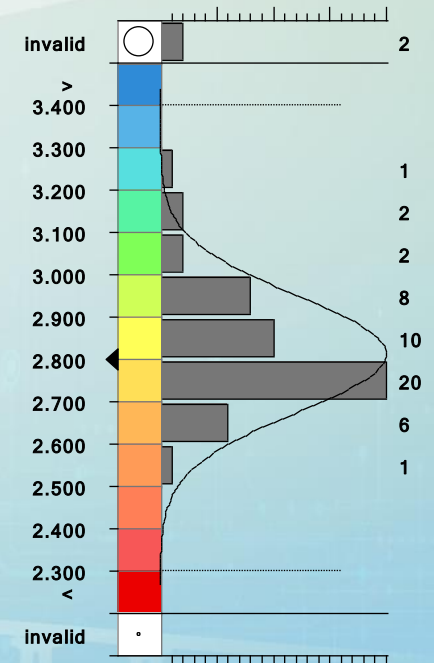
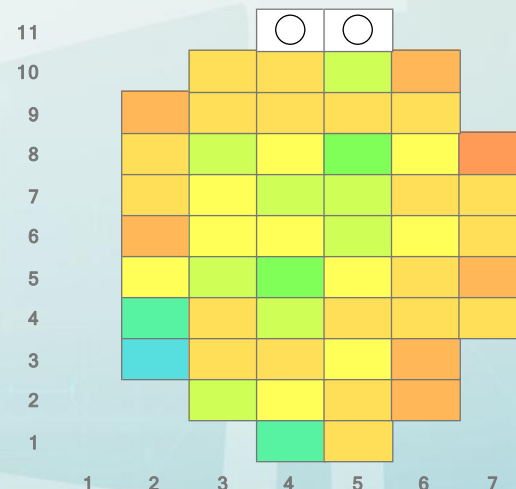
## Edge coupler



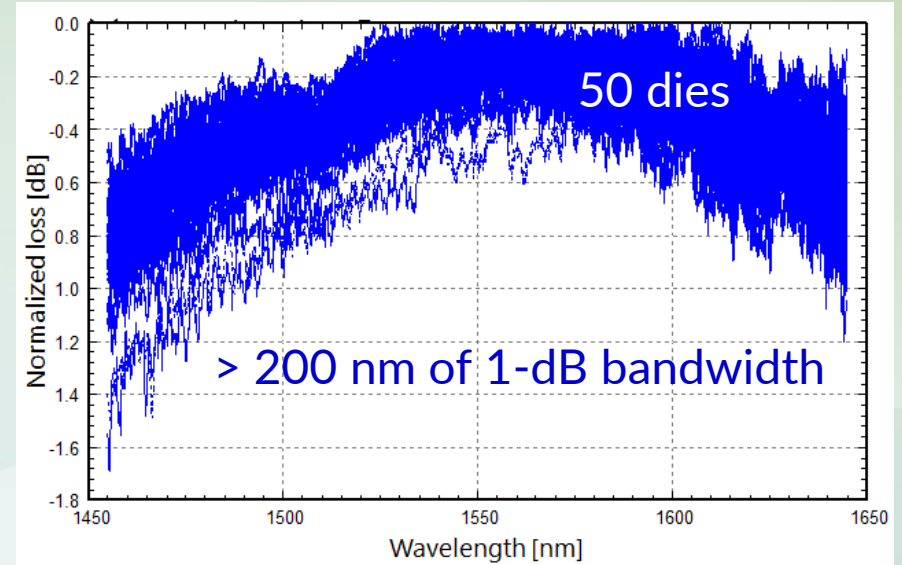
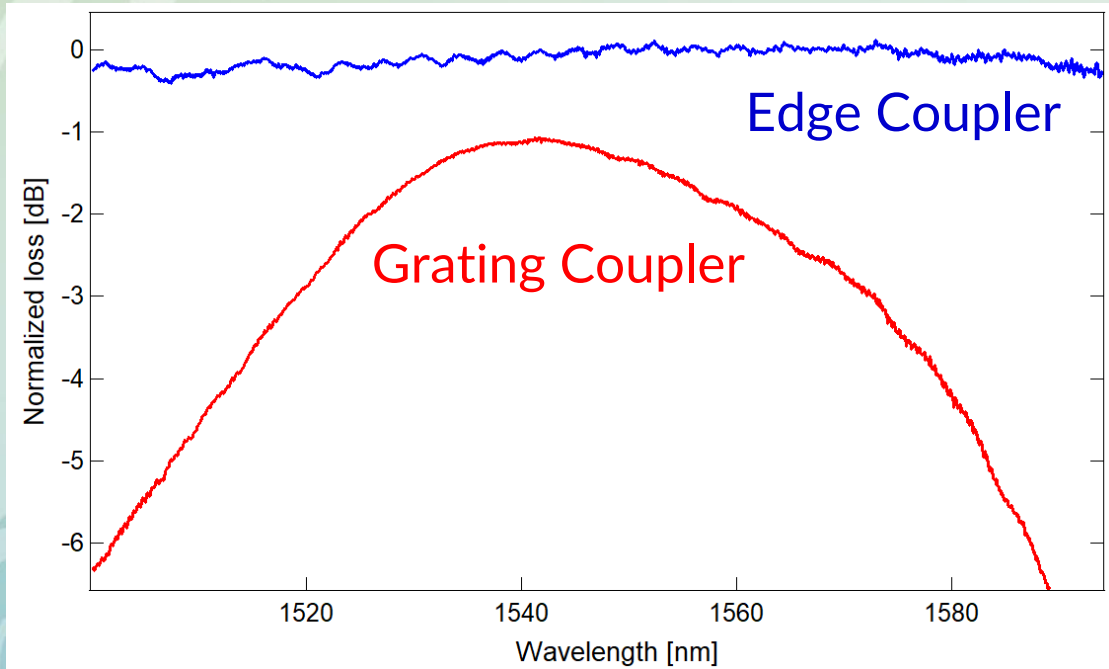
Mean coupling loss: 3.9 dB  $\pm$  0.2 dB



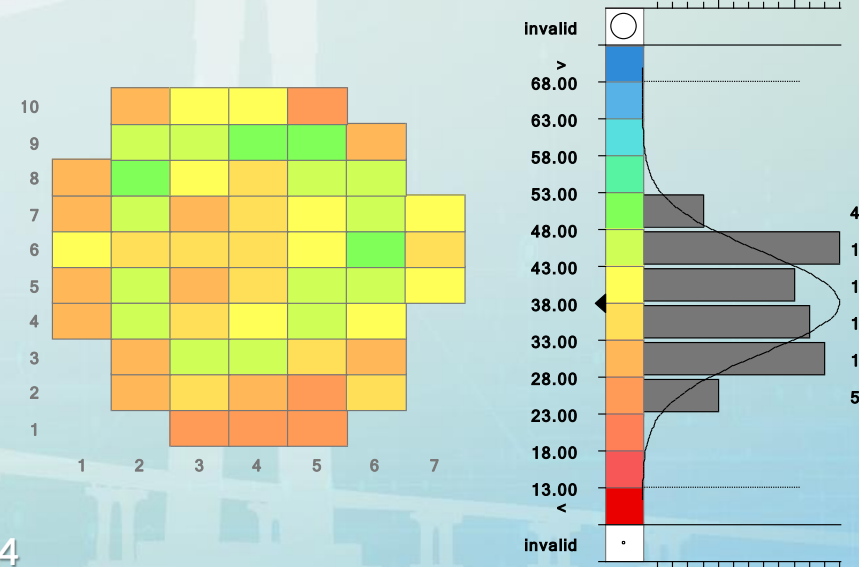
Mean coupling loss: 2.8 dB  $\pm$  0.1 dB



# Optical bandwidth Wafer level distribution



1-dB bandwidth  
of 38 nm ± 7nm  
(wafer variation)

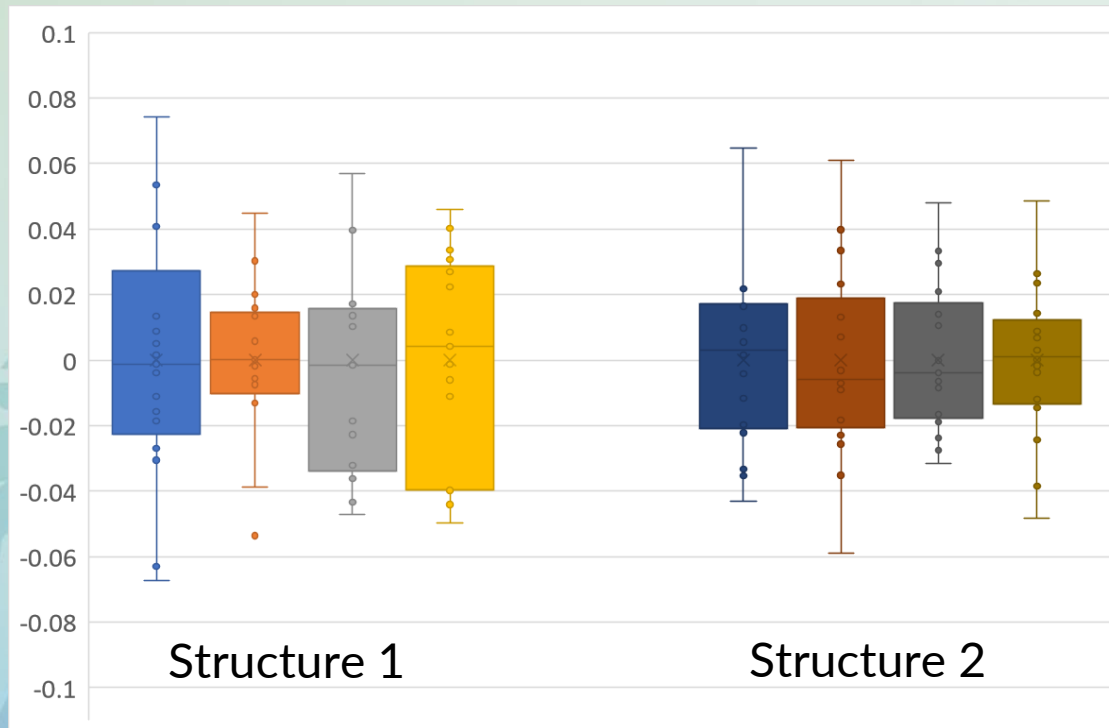


# Repeatability



## Coupling via grating coupler

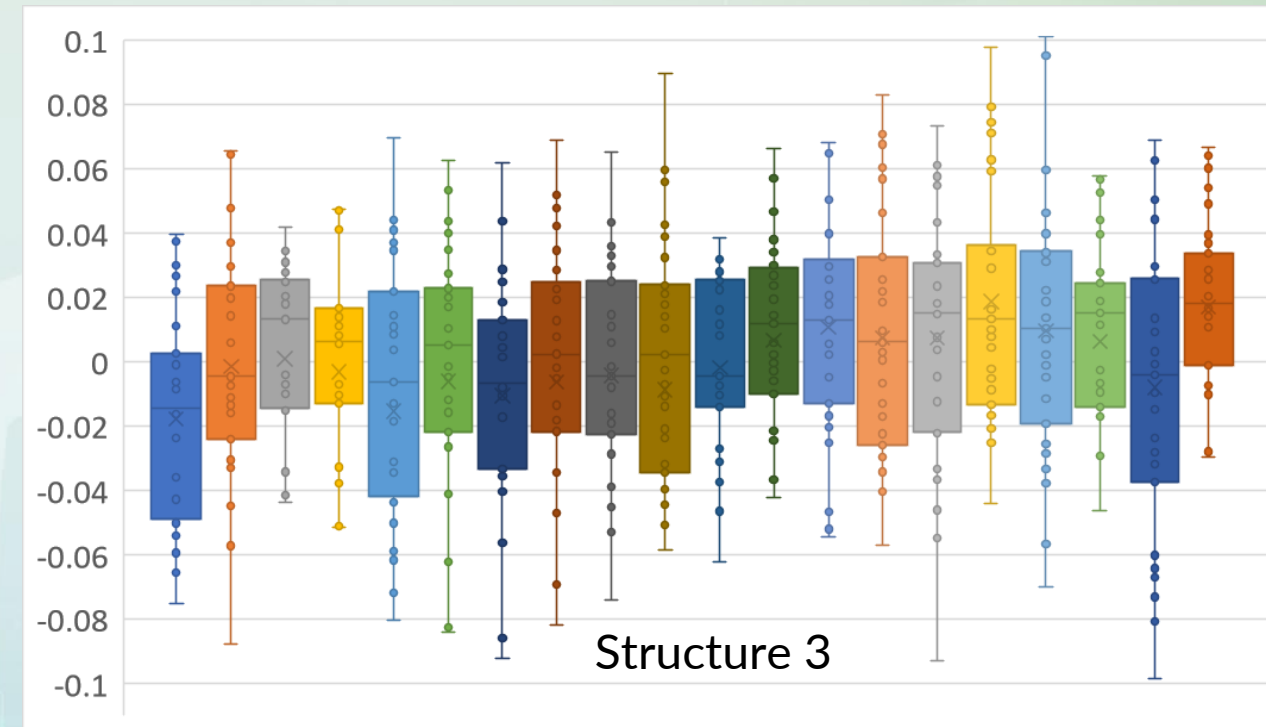
- over 4 dies
- 2 test structures
- repeated 17 times



$\sigma \sim 0.02$  dB

## Coupling via edge coupler

- over 31 dies
- 1 test structure
- repeated 20 times

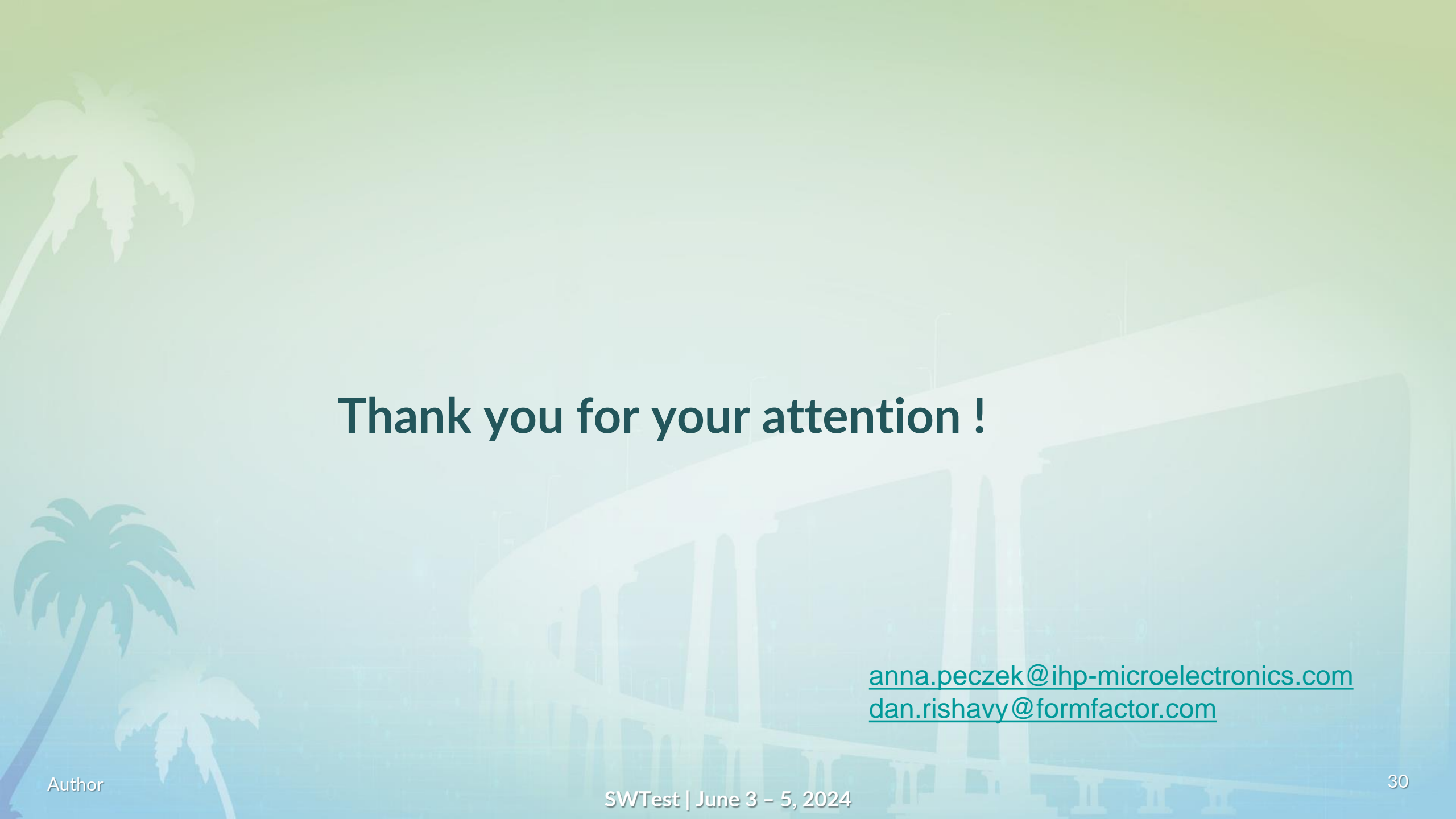


$\sigma \sim 0.02$  dB

# Measurement time

# Summary

- **Fully automated edge coupling was demonstrated on 200 mm wafer**
- **The system includes advanced, automated calibration routines for high accuracy PIC characterization**
- **Comparison with established grating coupler probing shows no significant drawback.**

The background of the slide features a light blue and green gradient. On the left side, there are three stylized palm tree silhouettes in shades of green and blue. The right side of the background shows a faint, semi-transparent image of a modern building with large windows and a curved facade.

**Thank you for your attention !**

[anna.peczek@ihp-microelectronics.com](mailto:anna.peczek@ihp-microelectronics.com)  
[dan.rishavy@formfactor.com](mailto:dan.rishavy@formfactor.com)